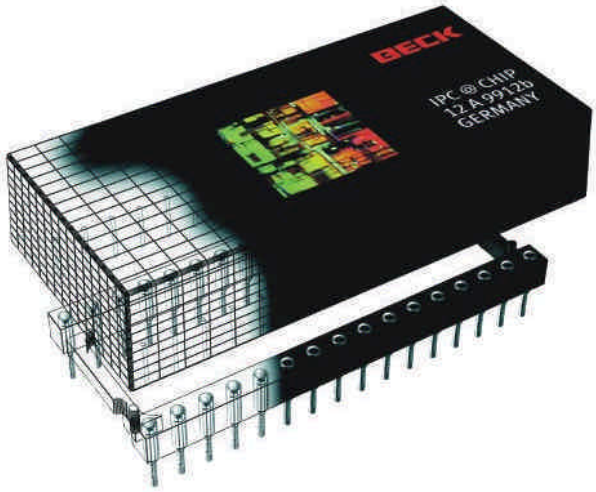


Preliminary

Hardware Manual

High Performance, 80186- and 80188-Compatible, 16-Bit Embedded Microcontroller Single Chip PC with Ethernet 10Base-T

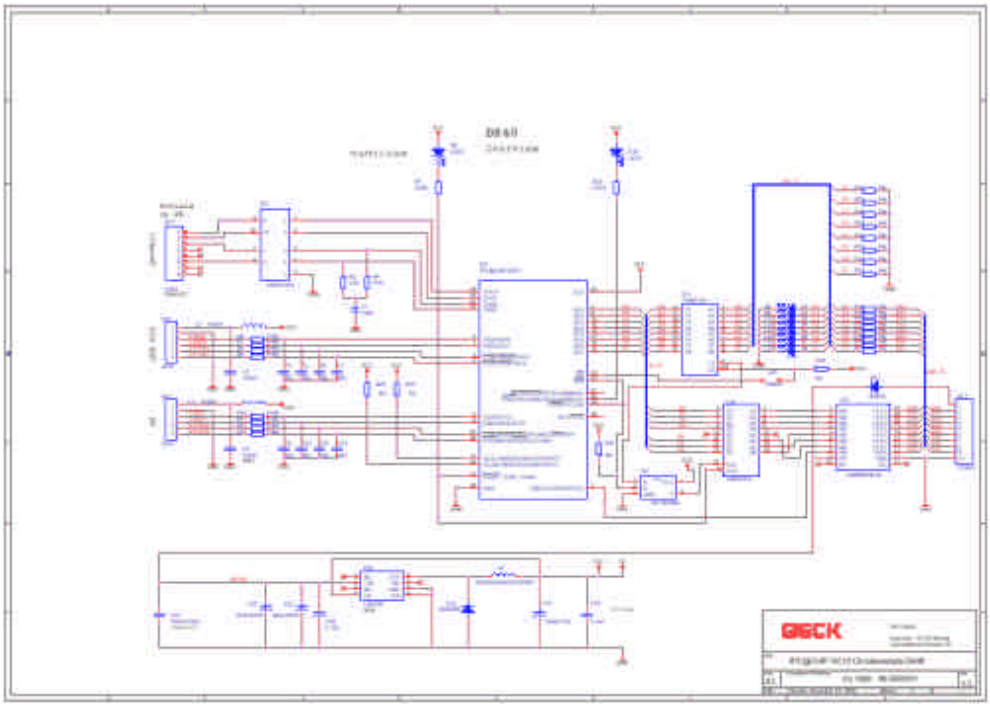


Table of Contents

1. BASIC SPECIFICATIONS

@CHIP	CPU	RAM	FLASH	Ethernet
SC01	80188 20MHz	128 Kbyte	128 Kbyte	No
SC02	80188 20MHz	128 Kbyte	128 Kbyte	10Base-T
SC11	80186 20MHz	512 Kbyte	512 Kbyte	No
SC12	80186 20MHz	512 Kbyte	512 Kbyte	10Base-T

IPC@CHIP® family 80186- and 80188-compatible microcontroller with up to 512KB-RAM, 512KB-Flash and Ethernet on Chip
- Lower system cost with higher performance

High performance
- 20-MHz operating frequencies
- Zero-wait-state operation at 20 MHz
- 1-Mbyte internal memory space
- 6 x 256-byte I/O space
- Low-power CMOS process with single 5V power supply

Enhanced integrated peripherals
- 14 programmable I/O (PIO) pins
- Two full-featured asynchronous serial ports allow full-duplex, 7-bit, 8-bit, or 9-bit data transfers, Serial port hardware handshaking with CTS,RTS, ENRX, and RTR selectable for each port
  Improved serial port operation enhances 9-bit DMA support
  Independent serial port baud rate generators
  DMA to and from the serial ports
- Ethernet controller for IEEE 802.3, 10Base-T,
  Integrated 10Base-T transceiver (SC02 and SC12 only)
  Auto-Polarity detection and correction
  Loopback capability for diagnostics
  Receiver and collision squelch circuit to reduce noise
  Built-in pre-distortion resisters for 10Base-T application
- Watchdog timer
- Pulse-width demodulation option
- Reset configuration register

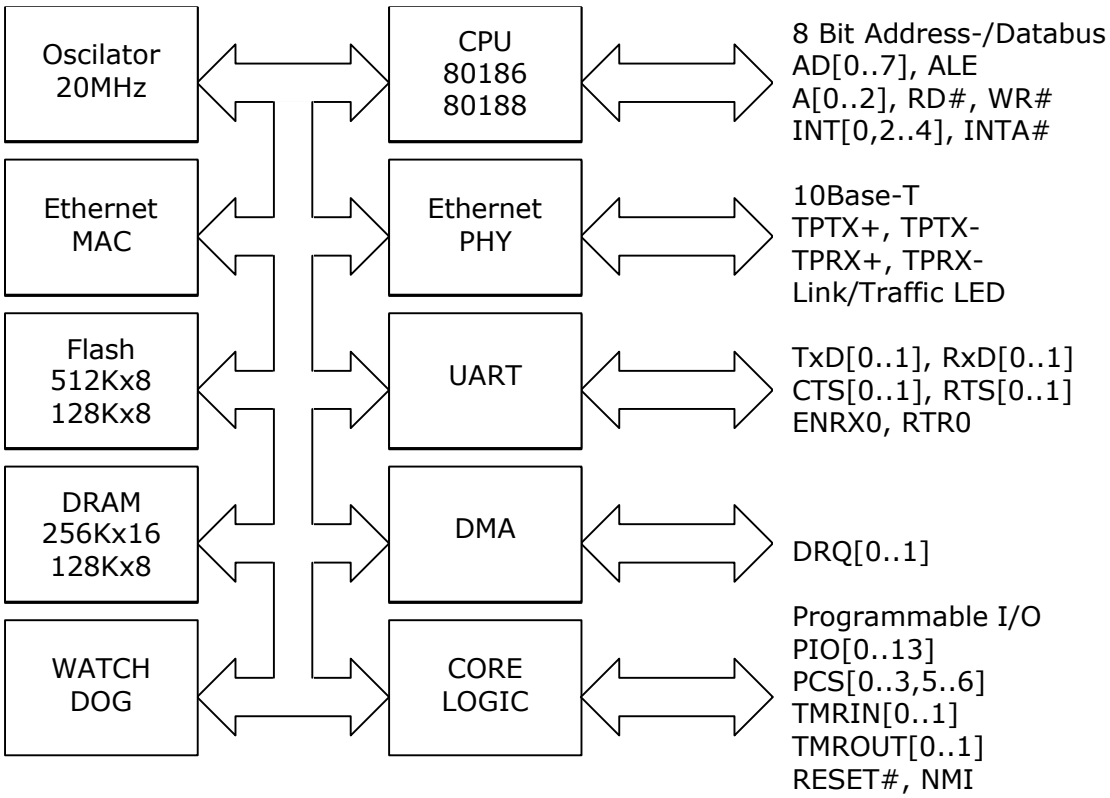
Familiar 80C186 peripherals
- Two independent DMA channels
- Programmable interrupt controller with up to six external and eight internal interrupts
- Three programmable 16-bit timers
- Programmable memory and peripheral chip-select logic

Software-compatible with the 80C186 and 80C188 microcontrollers with widely available native development tools, applications, and system software

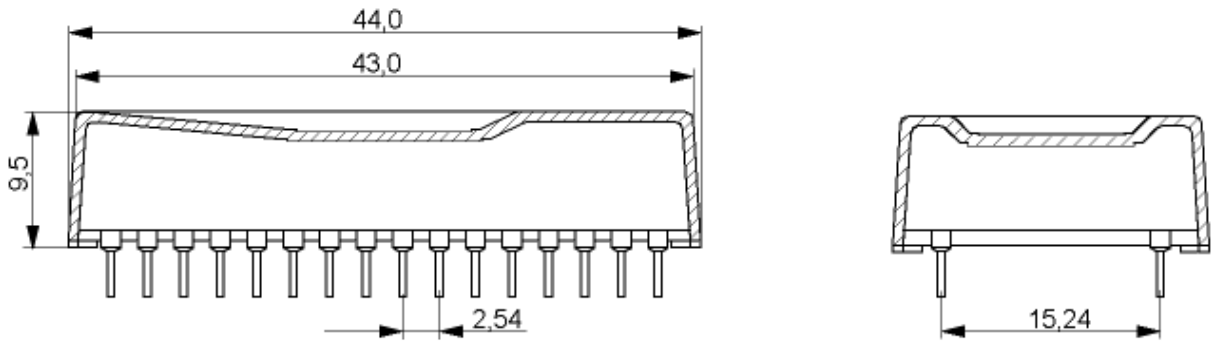
Available in the following packages:
- 32-pin, plastic pack (DIL32)

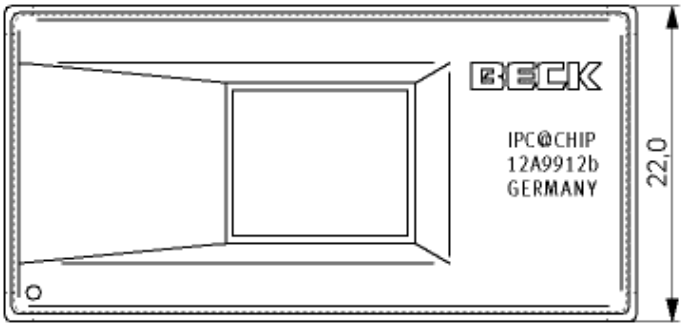
The @CHIP SC01/SC02/SC11/SC12 microcontrollers are part of the Beck IPC@CHIP® family of System on Chip microcontrollers and microprocessors based on the x86 architecture. The IPC@CHIP® family microcontroller is the ideal upgrade for 80C186/188 designs requiring 80C186/188 compatibility, increased performance, serial communications, Ethernet communications, a direct bus inter-face, and more than 64K of memory.
The IPC@CHIP® family microcontrollers integrates up to 512Kbyte DRAM with increased performance and up to 512Kbyte FLASH in reducing memory subsystem costs.
The IPC@CHIP® family microcontrollers also integrates the functions of the CPU, multiplexed address bus, three timers, watchdog timer, chip selects, interrupt controller, two DMA controllers, two asynchronous serial ports, programmable bus sizing, and pro-grammable I/O (PIO) pins on one chip.
The @CHIP SC11/SC12 microcontroller is a highly integrated design that provides all Media Access Control (MAC) and Encode-Decode (ENDEC) functions in accordance with the IEEE 802.3 standard. Network interfaces including 10Base-T via the Twisted-pair. The integrated 10Base-T transceiver makes @Chip SC11/SC12 more cost-effective.
Compared to the 80C186/188 microcontrollers, the IPC@CHIP® family microcontrollers enables designers to reduce the size, power consumption, and cost of embedded systems, while increasing reliability, functionality, and performance.
The IPC@CHIP® family microcontrollers has been designed to meet the most common requirements of embedded products developed for the communications, office automation, mass storage, and general embedded markets. Specific applications including industrial controls, data collection, protocoll conversion, process monitoring and internet connectivity.

IPC@CHIPâ family microntroller block diagram

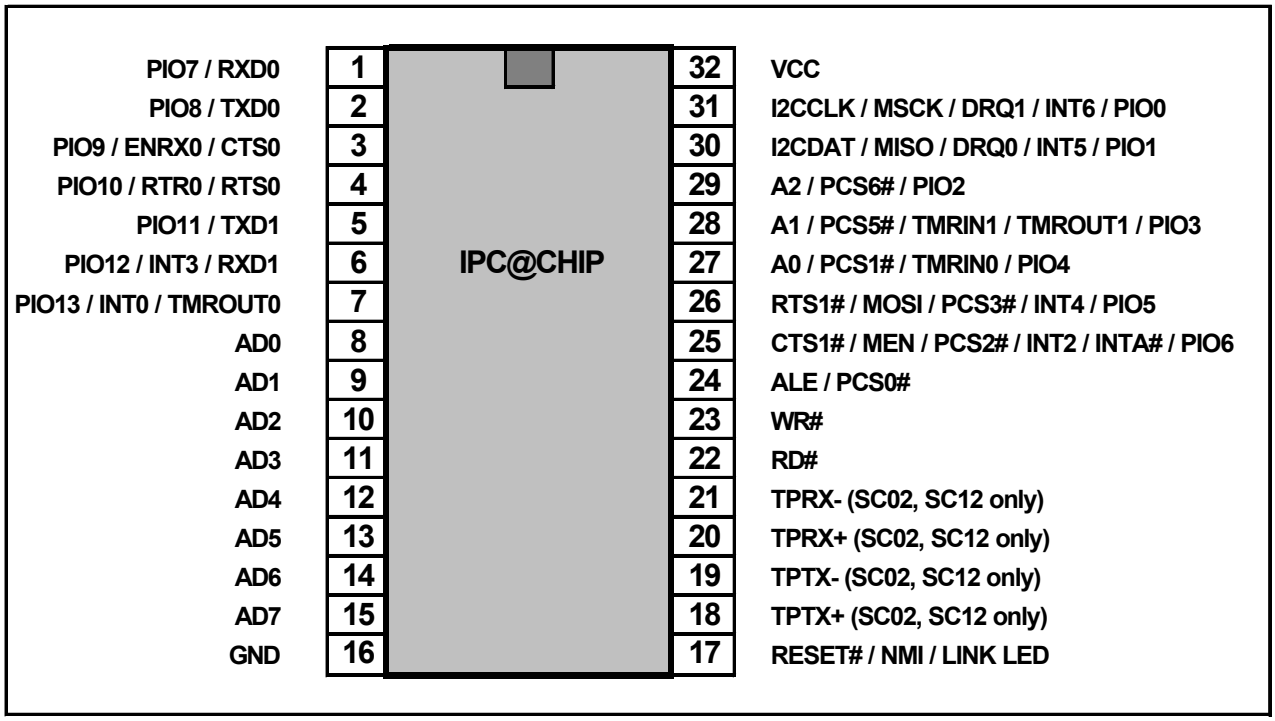


2. PHYSICAL DIMENSIONS





3. PIN CONFIGURATION



4. PIN FUNCTIONS

Pins That Are Used by Emulators
The following pins are used by emulators for debugging purposes: TxD0, RxD0

Pin Terminology
The following terms are used to describe the pins:
Input (I) - An input-only pin.
Output (O) - An output-only pin.
Input/Output (I/O) - A pin that can be either input or output.
Synchronous - Synchronous inputs must meet setup and hold times in relation to CLK. Synchronous outputs are synchronous to CLK.
Asynchronous - Inputs or outputs that are asynchronous to CLK.

4.1 Address / Data bus

Pin Name	Type	Function
A[0..2]	O	**Address Bus (output, three-state, synchronous)** These pins supply nonmultiplexed memory or I/O addresses to the system one half of a CLK period earlier than the multiplexed address and data bus (AD7–AD0). During a bus hold or reset condition, the address bus is in a high-impedance state. While the IPC@CHIP® family microntroller directly interfacing DRAM, A2–A0 will serve as the nonmultiplexed address bus for external SRAM, FLASH, PROM, EPROM, and peripherals.
AD[0..7]	I/O	**Multiplexed Address and Data Bus (input/output, three-state, synchronous, level-sensitive)** These time-multiplexed pins supply partial memory or I/O addresses, as well as data, to the system. This bus supplies the low-order 8 bits of an address to the system during the first period of a bus cycle (t1), and it supplies data to the system during the remaining periods of that cycle (t2 , t3 , and t4). In 8-bit mode, AD7–AD0 supplies the data for both high and low bytes. The address phase of these pins can be disabled. During a bus hold or reset condition, the address and data bus is in a high-impedance state.
ALE	O	**Address Latch Enable (output, synchronous)** This pin indicates to the system that an address appears on the address and data bus (AD7–AD0). The address is guaranteed to be valid on the trailing edge of ALE. This pin is three-stated during ONCE mode. ALE is three-stated and held resistively Low during a bus hold condition. In addition, ALE has a weak internal pulldown resistor that is active during reset, when it is enabled by software.
RD#	O	**Read Strobe (output, synchronous, three-state)** This pin indicates to the system that the microcontroller is performing a memory or I/O read cycle. RD is guaranteed to not be asserted before the address and data bus is floated during the address-to-data transition. RD floats during a bus hold condition.
WR#	O	**Write Strobe (output, synchronous)** This pin indicates to the system that the data on the bus is to be written to a memory or I/O device. WR floats during a bus hold or reset condition.

4.2 Programmable I/O Pins

Pin Name	Type	Function
PIO[0..13]	I/O	**Programmable I/O Pins (input/output, asynchronous, open-drain)** The IPC@CHIP® family microcontroller provides 14 individually programmable I/O pins. Each PIO can be programmed with the following attributes: PIO function (enabled/disabled), direction (input/output), and weak pullup or pulldown.

PIO ##	After power-on reset, the PIO pin defaults to	programmable as Input with
0	Input without	pullup
1	Input without	pullup
2	PCS6#	pullup
3	Input with pullup	pullup / pulldown
4	Input with pullup	pullup
5	Output high	pullup
6	Input with pullup	pullup
7	RxD0	pullup
8	TxD0	pullup
9	Input with pullup	pullup
10	Output high	pullup
11	TxD1	pullup
12	RxD1	pullup
13	Output low	pulldown

4.3 Programmable Chip Selects

Pin Name	Type	Function
PCS[0..3]	O	**Peripheral Chip Selects (output, synchronous)** These pins indicate to the system that an I/O memory access is in progress to the corresponding region of the peripheral memory. PCS3–PCS0 are three-stated and held resistively High during a bus hold condition. In addition, PCS3–PCS0 each have a weak internal pullup resistor that is active during reset. The PCS outputs assert with the multiplexed AD address bus. Note also that each peripheral chip select asserts over a 256-byte address range, which is twice the address range covered by peripheral chip selects in the 80C186 and 80C188 microcontrollers. PCS3–PCS0 also have extended wait state options, default is 15 wait states.
PCS[5..6]	O	**Peripheral Chip Selects (output, synchronous)** These pins indicate to the system that an I/O memory access is in progress to the corresponding region of the peripheral memory. PCS6–PCS5 are three-stated and held resistively High during a bus hold condition. In addition, PCS6–PCS5 each have a weak internal pullup resistor that is active during reset. The PCS outputs assert with the multiplexed AD address bus. Note also that each peripheral chip select asserts over a 256-byte address range, which is twice the address range covered by peripheral chip selects in the 80C186 and 80C188 microcontrollers. PCS6–PCS6 also have extended wait state options, default is 3 wait states, on SC02 and SC12 changing is not allowed.

4.4 Interrupts

Pin Name	Type	Function
INT[0,2-4]	I	**Maskable Interrupt Request (input,asynchronous)** These pins indicate to the microcontroller that an interrupt request has occurred. If the INT pin is not masked, the microcontroller transfers program execution to the location specified by the corresponding INT vector in the microcontroller interrupt vector table. Interrupt requests are synchronized internally and can be edge-triggered or level-triggered. To guarantee interrupt recognition, the requesting device must continue asserting INT until the request is acknowledged. INT2 becomes INTA when INT0 is configured in cascade mode.
INTA#	O	**Interrupt Acknowledge (output, synchronous)** When the microcontroller interrupt control unit is operating in cascade mode, this pin indicates to the system that the microcontroller needs an interrupt type to process the interrupt request on INT0. The peripheral issuing the interrupt request must provide the microcontroller with the corresponding interrupt type.
PWD		**Pulse Width Demodulator (input, Schmitt trigger)** If pulse width demodulation is enabled, PWD processes a signal through the Schmitt trigger. PWD is used internally to drive TMRIN0 and INT2, and PWD is inverted internally to drive TIMERIN1 and INT4. If INT2 and INT4 are enabled and timer 0 and timer 1 are properly configured, the pulse width of the alternating PWD signal can be calculated by comparing the values in timer 0 and timer 1. In PWD mode, the signals TMRIN0, TMRIN1 and INT4 can be used as PIOs. If they are not used as PIOs, they are ignored internally.

4.5 Timer

Pin Name	Type	Function
TMRIN[0..1]	I	**Timer Input (input, synchronous, edge-sensitive)** These pins supply a clock or control signal to the internal microcontroller timer 0 and 1. After internally synchronizing a Low-to-High transition on TMRIN, the microcontroller increments the corresponding timer. TMRIN must be tied High if not being used. When PIO is enabled, TMRIN is pulled High internally. TMRIN0 is driven internally by INT2/PWD when pulse width demodulation mode is enabled. The TMRIN0 pin can be used as a PIO when pulse width demodulation mode is enabled.
TMROUT[0..1]	O	**Timer Output (output, synchronous)** These pins supplies the system with either a single pulse or a continuous waveform with a programmable duty cycle. TMROUT is floated during a bus hold or reset.

4.6 10Base-T Interface

Pin Name	Type	Function
TPTX[+,-]	O	**Twisted Pair Driver (outputs)** These two outputs provide the TP drivers with pre-distortion capability
TPRX[+,-]	I	**Twisted Pair Receive (inputs).** A differential receiver tied to the receive transformer pair of the twisted-pair wire. The receive pair of the twisted-pair medium is driven with 10 Mbits/s Manchester-encoded data
LINK LED	O	**Link and Traffic LED Driver (output)** If TP is LINK-pass, this pin outputs 2.5V. This pin will output 5V for 80ms to indicate the presence of traffic on the network. If no LED / 200Ω combination is connexted to this pin, 1K pullup should be tied to this pin, to make shure RESET# and NMI function is available.

4.7 Asynchronous Serial Ports

Pin Name	Type	Function
TxD[0..1]	O	**Transmit Data (output, asynchronous)** These pins supply asynchronous serial transmit data to the system from serial port 0 and 1.
RxD[0..1]	I	**Receive Data (input, asynchronous)** These pins supply asynchronous serial receive data from the system to asynchronous serial ports 0 and 1.
CTS[0..1]	I	**Clear-to-Send (input, asynchronous)** These pins provide the Clear-to-Send signal for asynchronous serial port 0 and 1 when hardware flow control is enabled for the port. The CTS signals gate the transmission of data from the associated serial port transmit register. When CTS is asserted, the transmitter begins transmission of a frame of data, if any is available. If CTS is deasserted, the transmitter holds the data in the serial port transmit register. The value of CTS is checked only at the beginning of the transmission of the frame.
ENRX0	I	**Enable-Receiver-Request 0 (input, asynchronous)** This pin provides the Enable Receiver Request for asynchronous serial port 0 when hardware flow control is enabled for the port. The ENRX0 signal enables the receiver for the associated serial port.
RTS[0..1]	O	**Ready-to-Send 0 (output, asynchronous)** These pins provide the Ready-to-Send signal for asynchronous serial ports 0 and 1 when hardware flow control is enabled for the port. The RTS signals are asserted when the associated serial port transmit register contains data that has not been transmitted.
RTR0	O	**Ready-to-Receive 0 (output, asynchronous)** This pin provides the Ready-to-Receive signal for asynchronous serial port 0 when hardware flow control is enabled for the port. The RTR0 signal is asserted when the associated serial port receive register does not contain valid, unread data.

4.8 DMA

Pin Name	Type	Function
DRQ[0..1]	I	**DMA Request (input, synchronous, level-sensitive)** These pins indicate to the microcontroller that an external device is ready for DMA channel 0 or 1 to perform a transfer. DRQ0 is edge-triggered and internally synchronized. DRQ is not latched and must remain active until serviced.

4.9 Synchronous Peripheral Interface (SPI)

Pin Name	Type	Function
MEN	O	**Not implemented yet**
MSCK	O	**Not implemented yet**
MISO	I	**Not implemented yet**
MOSI	O	**Not implemented yet**

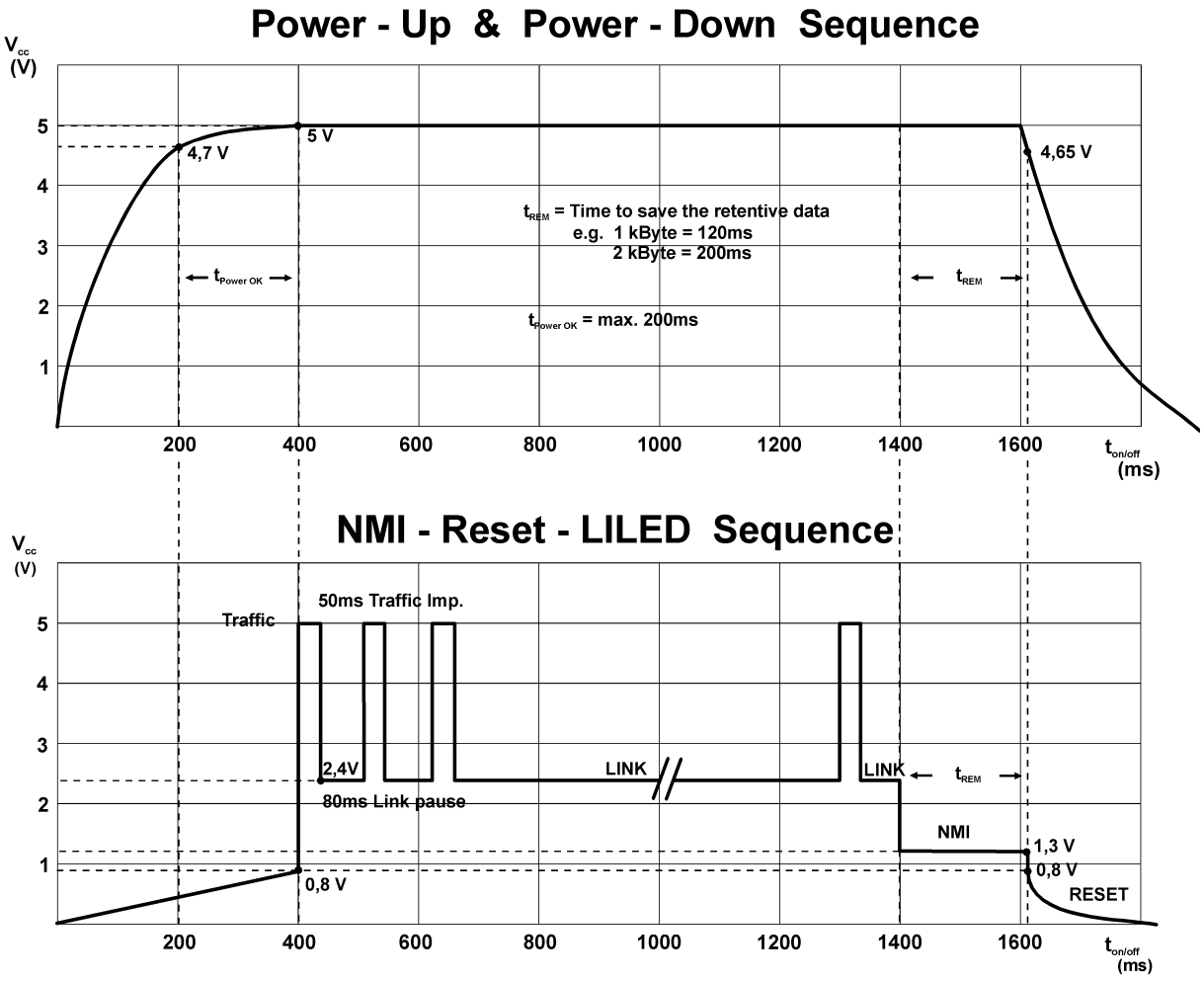
4.10 I^2C-Bus

Pin Name	Type	Function
I^2CCLK	O	**I^2C-Bus Clock (output)** This pin provides clock to an external I^2C slave.
I^2CDAT	I/O	**I^2C-Bus Data in/out (input/output)** This pin acts either as data input or data output. The IPC@CHIP® family microntroller handles up to 127 external slaves. Itself is always master and cannot addressed as slave.

4.11 Reset, Power Fail Generator

Pin Name	Type	Function
RESET#	I/O	**Reset (input/output, asynchronous, level-sensitive)** If voltage on this pin goes down below 0.8V this pin requires the microcontroller to perform a reset. When RESET is asserted, the microcontroller immediately terminates its present activity, clears it's internal logic, and transfers CPU control to the reset address, FFFF0h. If Vcc goes down below 4.5V or internal watchdog is released this pin will be driven to GND.
NMI	I	**Nonmaskable Interrupt (input, synchronous, edge-sensitive)** If voltage on this pin goes down below 1.5V it indicates to the microcontroller that an interrupt request has occurred. The NMI signal is the highest priority hardware interrupt and, unlike the INT6–INT0 pins, cannot be masked. The microcontroller always transfers program execution to the location specified by the nonmaskable interrupt vector in the microcontroller interrupt vector table when NMI is asserted. Although NMI is the highest priority interrupt source, it does not participate in the priority resolution process of the maskable interrupts. There is no bit associated with NMI in the interrupt in-service or interrupt request registers. This means that a new NMI request can interrupt an executing NMI interrupt service routine. As

		with all hardware interrupts, the IF (interrupt flag) is cleared when the processor takes the interrupt, disabling the maskable interrupt sources. However, if maskable interrupts are re-enabled by software in the NMI interrupt service routine, via the STI instruction for example, the fact that an NMI is currently in service does not have any effect on the priority resolution of maskable interrupt requests. For this reason, it is strongly advised that the interrupt service routine for NMI should not enable the maskable interrupts. An NMI transition from Low to High is latched and synchronized internally, and it initiates the interrupt at the next instruction boundary. To guarantee that the interrupt is recognized, the NMI pin must be asserted for at least one CLK period.



5. FUNCTIONS THAT ARE MUTUAL EXCLUSIVE

The IPC@CHIP® family microcontroller provides a lot of different functions by several multi-function pins. Choosing one function will result in disabling other functions. The following table shows, which functions are mutual exclusive.

Pin Name	Function	Exclusion
A0	nonmultiplexed address A0	PIO4, PCS1#, TMRIN0
A[1..2]	nonmultiplexed address A[1..2]	PIO[2..3], PCS[5..6], Timer 1
ALE	Address / Data bus	PCS0#
CTS0 / ENRX0#	hardware flow control Serial Port 0	PIO9
CTS1	hardware flow control Serial Port 1	PIO6, PCS2#, INT2, INTA#, PWD, SPI
DRQ0	DMA Request 0	PIO1, INT5, I^2C-Bus, SPI
DRQ1	DMA Request 1	PIO0, INT6, I^2C-Bus, SPI
I^2CCLK, I^2CDAT	I^2C-Bus	PIO[0..1], DMA, INT[5..6], SPI
INT0	Interrupt Request 0	PIO13, TMROUT0, cascaded Interrupt Controller
INT0	cascaded Interrupt Controller	PIO6, PIO13, INT2, PCS2#, PWD, SPI, TMROUT0, hw flow control Serial Port 1
INT2	Interrupt Request 2	PIO6, PCS2#, INTA#, PWD, SPI, hardware flow control Serial Port 1
INT3	Interrupt Request 3	PIO12, Serial Port 1
INT4	Interrupt Request 4	PIO5, PCS3#, SPI, hardware flow control Serial Port 1
INT5	Interrupt Request 5	PIO1, DRQ0, I^2C-Bus, SPI
INT6	Interrupt Request 6	PIO0, DRQ1, I^2C-Bus, SPI
INTA#	cascaded Interrupt Controller	PIO6, PIO13, INT0, INT2, PCS2#, PWD, TMROUT0, SPI, hw flow control Serial Port 1
PCS0#	programmable chip select 0	Address/Data bus
PCS1#	programmable chip select 1	A0, PIO4, TMRIN0, SPI
PCS2#	programmable chip select 2	PIO6, INT2, INTA#, PWD, SPI, hw flow control Serial Port 1, cascaded Interrupt Controller
PCS3#	programmable chip select 3	PIO5, INT4, SPI, hardware flow control Serial Port 1
PCS5#	programmable chip select 5	A[1..2], PIO3, Timer 1
PCS6#	programmable chip select 6	A[1..2], PIO2

continued on next page ...

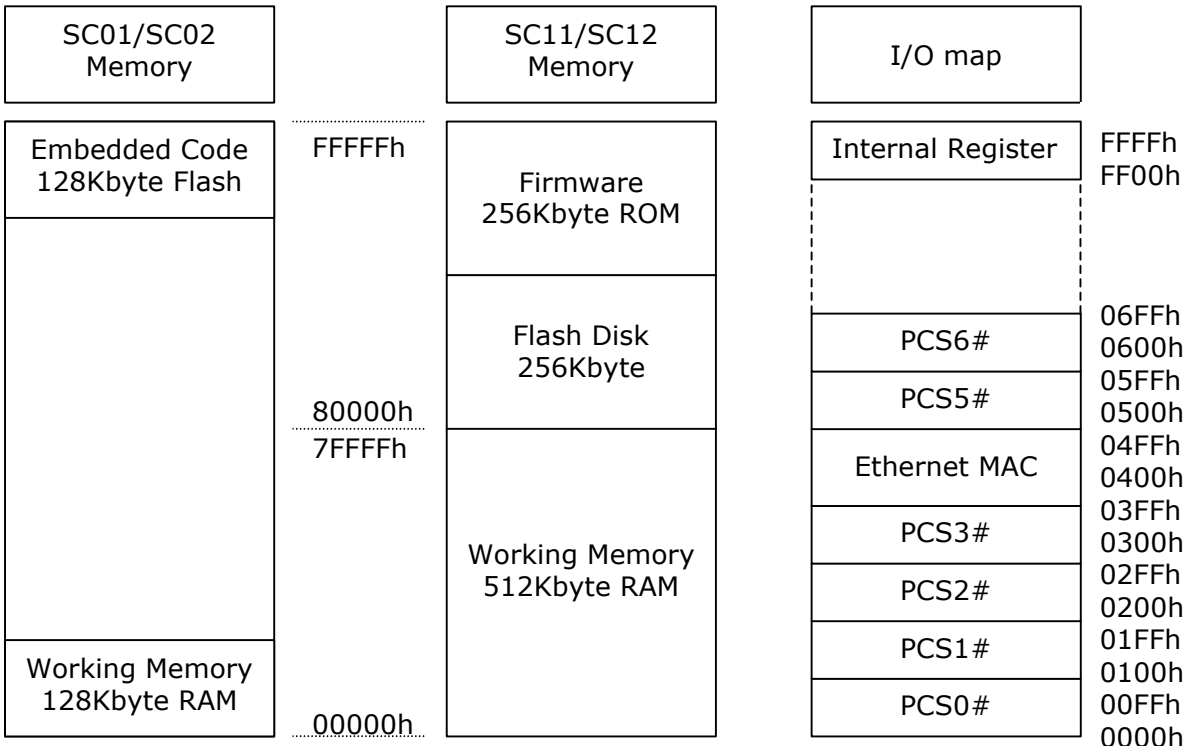
Pin Name	Function	Exclusion
PIO0	programmable I/O	DRQ1, INT6, I^2C-Bus, SPI
PIO1	programmable I/O	DRQ0, INT5, I^2C-Bus, SPI
PIO2	programmable I/O	A2, PCS6#
PIO3	programmable I/O	A1, PCS#, Timer 1
PIO4	programmable I/O	A0, PCS1#, TMRIN0, SPI
PIO5	programmable I/O	PCS3#, INT4, SPI, hardware flow control Serial Port 1
PIO6	programmable I/O	PCS2#, INT2, cascaded Interrupt Controller, PWD, SPI, hw flow control Serial Port 1
PIO7	programmable I/O	Serial Port 0
PIO8	programmable I/O	Serial Port 0
PIO9	programmable I/O	hardware flow control Serial Port 0
PI1O	programmable I/O	hardware flow control Serial Port 0
PI11	programmable I/O	Serial Port 1
PI12	programmable I/O	Serial Port 1, INT3
PI13	programmable I/O	INT0, cascaded Interrupt Controller, TMROUT0
RxD0, TxD0	Serial Port 0 w/o hw flow control	PIO[7..8]
RxD0, TxD0 CTS0, RTS0	Serial Port 0 with hw flow control	PIO[7..10]
RxD1, TxD1	Serial Port 1 w/o hw flow control	PIO[11..12], INT3
RxD1, TxD1 CTS1, RTS1	Serial Port 1 with hw flow control	PIO[5..6,11..12], INT3, PCS[2..3]#, INT2, INT4, PWD, SPI, cascaded Intrpt. Controller
MEN, MSCK MISO,MOSI	SPI (Synchronous Peripheral Intf.)	A0, PIO[0..1,4..5], PCS[1,3]#, INT[2,4..6], DMA, I^2C-Bus, PWD,TMRIN0, hw flow control Serial Port 1, cascaded Intrpt. Controller

6. SYSTEM OVERVIEW

IPC@CHIP® family microcontroller has a system configuration based on the ISA architecture with some changes: No ISA-Bus, no Video-Interface, no Keyboard Interface, programming of Serial Ports, DMA, PIC and Timer is different from standard IBM PC.

This section provides an overview of the system memory configuration and basic I/O.

6.1 Memory map



6.2 System interrupts

Interrupt Request 1 is internaly connected to Ethernet MAC and is not available extern.

7. CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

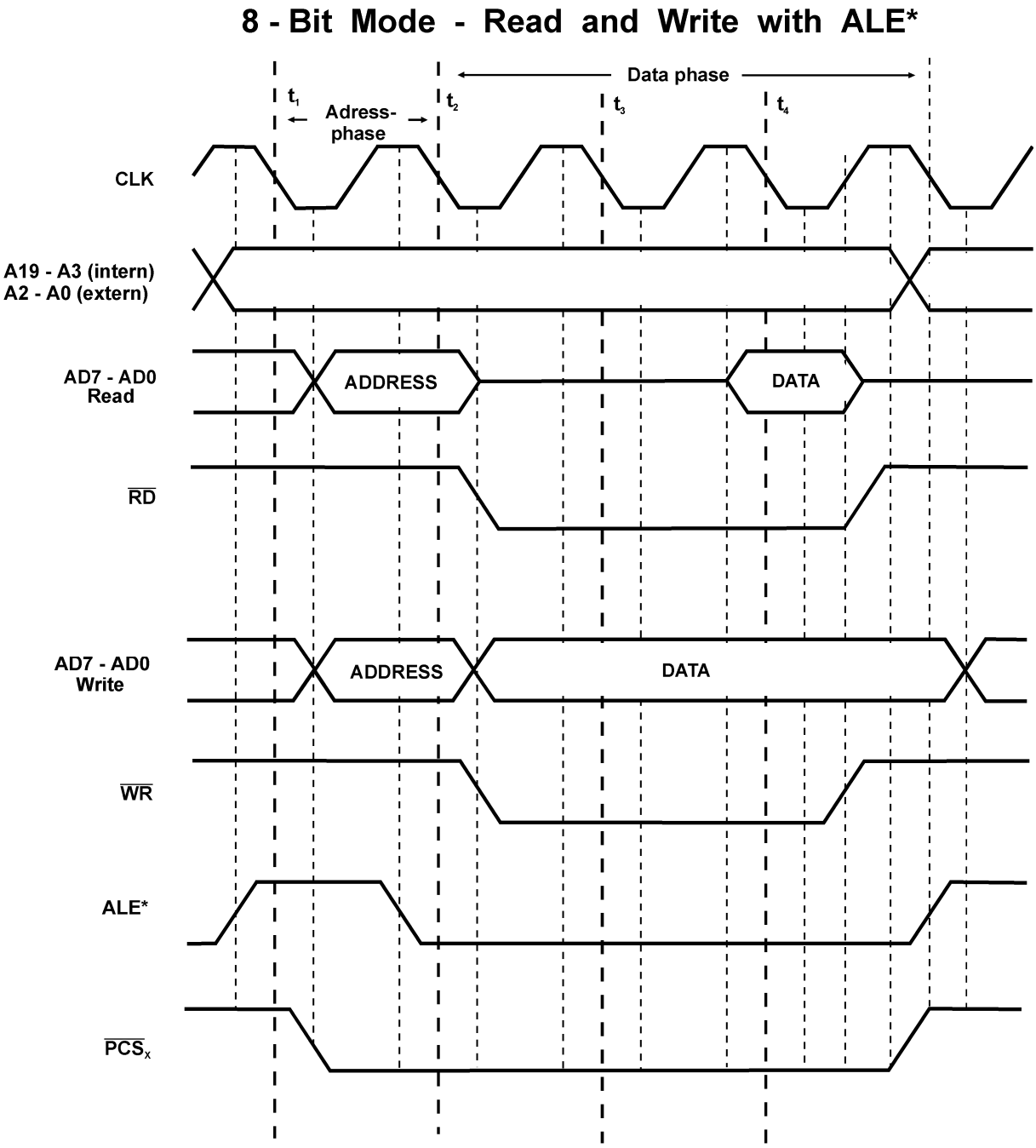
Storage temperature : -25°C to +70°C see IEC 68-2-1/2
Supply voltage (Vcc) : 5V +/- 10%
Supply current (Vcc = 5,5V) : 400 mA
Voltage on any pin with respect to ground : -0,5V to Vcc + 0,5V

OPERATING RANGES

Operating temperature (Case temp. tc) : 0°C to +55°C
Power supply current @ 20MHz : min. 350mA typ. 380mA max. 400mA

DC-CHARACTERISTICS

Symbol	Parameter Description	Test Condition	Preliminary		Unit
			MIN.	MAX.	
VOL	Voltage Output Low	IOL = 2.5mA	-	0.45	V
VOH	Voltage Output High	IOH = -2.4mA@2.4V IOH = -0.2mA@Vcc-0.5	2.4 Vcc-0.5	Vcc+0.5 Vcc	V V
VILO	Voltage Input Low	-	-0.5	Vcc-0.3	V
VIHI	Voltage Input High	-	2.0	Vcc+0.5	V
VRESLO	Voltage Reset Low	TTL level with Appl. 1	-	0.8	V
VRESHI	Voltage Reset High	TTL level with Appl. 1	2.4	Vcc+0.5	V
VPFNMI	Voltage Power fail	TTL level with Appl. 1	-	0.8	V
VCRT	Voltage Serial COM Receive & Transmit	TTL High TTL Low	2.4 -	Vcc+0.5 0.8	V V
VICDC	Voltage I²C Data & Clock	TTL High TTL Low	2.4 -	Vcc+0.5 0.8	V V
VTPRX	Voltage TP Receive	Input	0.35	2.0	V
VTPTX	Voltage TP Transmit	Output	0.8	2.4	V



*Address Bus - Latch - Enable

8. APPLICATION EXAMPLES

The following 5 pages contain schematics, showing the IPC@CHIP® family microcontroller in two applications (BECK-IPC GmbH: DK40 and FEC-FC34) and gives you three solutions, how to handle the multi-function pin 17 RESET# / NMI / LINK-LED.

DK40

Overview

Traffic/Link

Schield on PE

10BaseT

SYS EXT

PG

IC2 IPC@CHIP SC12

IC1 FS22101Y4

IC3 74ABT541

IC4 74ABT273

IC5 UDN2982SLW

IC6 LM2594 SO8

IC7 NC7S32M5

KL1 CON10

JP1 JUMP2

D9 LED2

D10 LED1

D11 1N4007

L2 100uH

L3 100uH

L4 220uH/500mA/DO3308P

D12 30BQ040

INT24V

C17 100nF/250V Capacitor

C21 22uF/35VS

C22 22uF/35VS

C19 0.1uF

C15 100uF/10V

C20 0.1uF

5V/500mA

BECK

IPC GmbH

Germany - 35578 Wetzlar
Garbenheimer Strasse 38

Title: IPC@CHIP SC12 Circuitexample DK40

Size: A3

Document Number: (c) 1996 - 99 DK40D1

Rev: 0.8

Date: Tuesday, November 23, 1999

Sheet 1 of 1

FC34

DC IN

ST3 — 980-S-3

BR1, JUMP2, BR2, JUMP2, V1, V2

IN24V, IN0V, PE

NETZTEIL 24V

REL24V, OUT24V, OUT0V

5V, 0V

VCC, GND

ST4 — 980-S-2

DC OUT

OUT RELAIS

ST2 — 980-S-11

A0.01.COM, A0.0, A0.1, A0.2, A0.3, A0.4, A0.5, A0.6, A0.7, A0.2-7.COM, A0.0-7.GND

FC34D1B
Ausgabe-Elektronik

RESET#, TMROUT0, D[0..15], WR#, PCS3#, DIAG, WD#, PCS0#, P10

FC34D1D

Eingabe-Elektronik

REL24V, OUT0V

E0.0, E0.1, E0.2, E0.3, E0.4, E0.5, E0.6, E0.7, E0.COM, E1.0, E1.1, E1.2, E1.3, E1.COM

ST5 — 980-S-14

IN NPN/PNP

TMRIN1, TMRIN0, INT2, INT4, INT2/PWD

E[0..7]

FC34D1A

10BaseT

Schirm auf PE

ST7

R6 0R

R7 0R

CON8
RJ45ST1

GND

IC24
SF1012
VALORSMD

R9 47R, R8 47R

C9 10nF, C8 10nF

IC?
IPC@CHIP SC12

TPTX+, TPTX-, TPRX+, TPRX-

TXD0/P8, RXD0/P7

CTS0/ENRX0/P9, RTS0/RTR0/P10

RD#, WR#

MCS0/PCS1/P4/TMRIN0/A0
PCS5/P3/TMROUT1/TMRIN1/A1
PCS6/P2/A2

TMRIN0, TMRIN1, PCS6#

TXD1/P11, RXD1/P12

ALE/PCS0, PCS0#

CTS1/MEN/PCS2/P6/INT2/INTA/PW
RTS1/MOSI/PCS3/P5/INT4

INT2/PWD, INT4

I2CCLK/MSCK/DRQ1/INT6/P0
I2CDAT/MISO/DRQ0/INT5/P1

RESET_PFAIL_LILED

GND, TMROUT0/INT0/P13, P10

AD0–AD7, D0–D7

IC?
74AHCT541

G1, G2, PCS0#, RD#

IC?
74HCT377

CLK, G

POWER
* GRUEN+ROT PG DOWNLOAD

IC15F 74HCT14 — R60 390E — D7
IC15E 74HCT14 — R61 390E — DUOLED, DUOLED5
IC15D 74HCT14 — R58 390E — D6 ERROR LED

SYS EXT

ST45 — RJ12

L30 100uH, VCC

ETXD0, ERXD0, ECTS0#, ERTS0#

R69–R72 100R

100nF, C36–C39 2n2

PG

ST1 — RJ12

L31 100uH, VCC

ETXD1, ERXD1

R? 100R, C? 2n2, 100nF

Traffic/Link

L1 LED, R62 470R

S? SW PFAIL, D? ZD1V4, S? SW MRESET

IC?A 74HCT14 — RESET — IC?A 74HCT14 — RESET#

R59 1K5, IC15A, TP1 TP10K, IC15B 74HCT14 — INT0

C18 2u2F/6V3 1206

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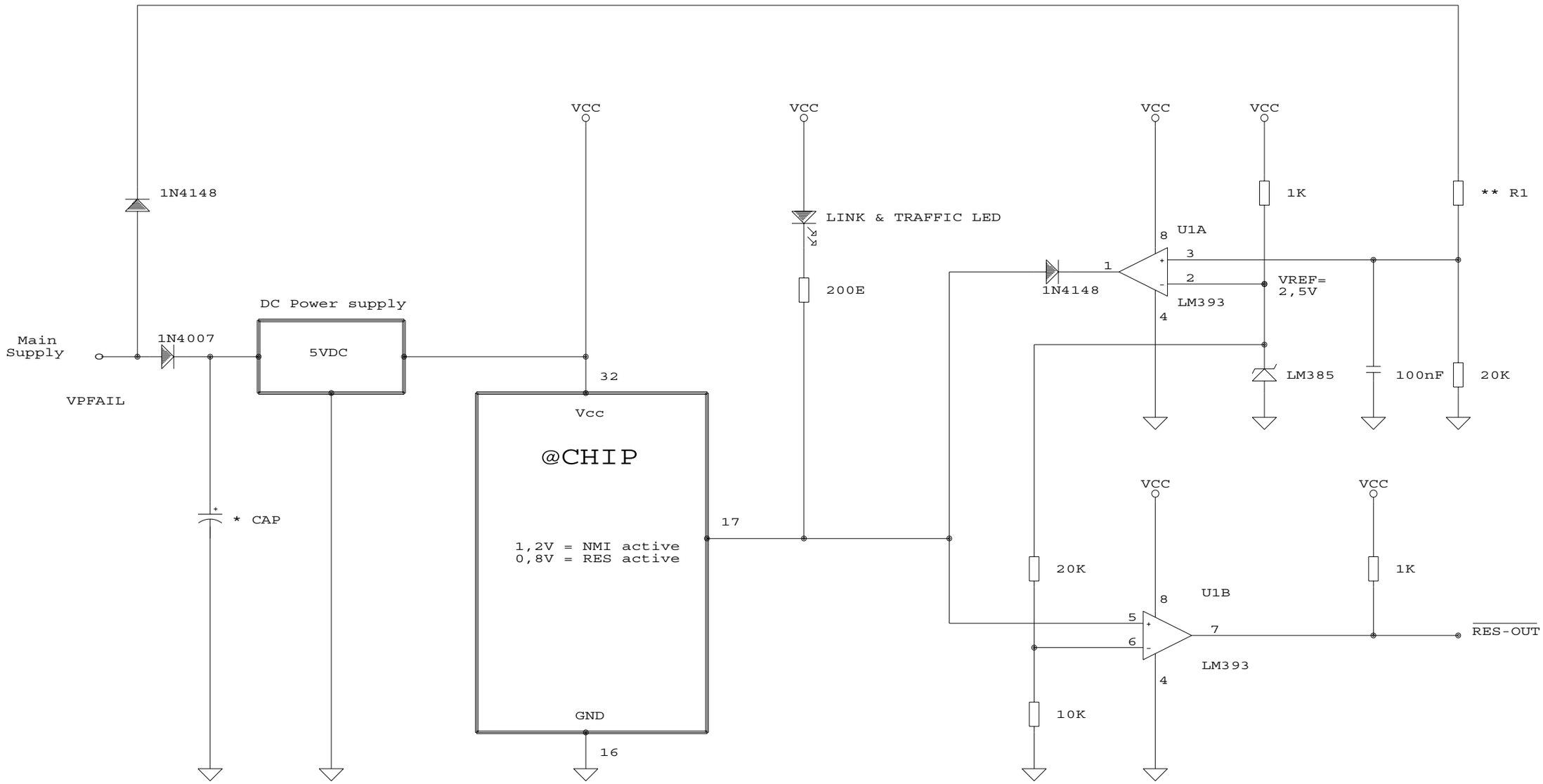
Title: IPC@CHIP SC12 circuit example (FC34 Rev. 1.1)

Size: A3 | Document Number: (c) 1996 - 99 CHIPD1 | Rev: 0.5

Date: Tuesday, November 23, 1999 | Sheet 1 of 1



PFAIL = Power Fail is used to monitor main supply voltage, not main Vcc+5VDC.
This is an Analog-Comparator-Input that activates NMI.

$\overline{\text{RES-OUT}}$ = LOW active Reset Out to any external Logik.

* CAP = Value is dependent from the saveable amount of data.

** R1 = $20000 * \left[\frac{VPFAIL - 0,7V}{2,5V} - 1 \right]$

Gez. : IB 16.11.99
Gepr.: JW 15.11.99

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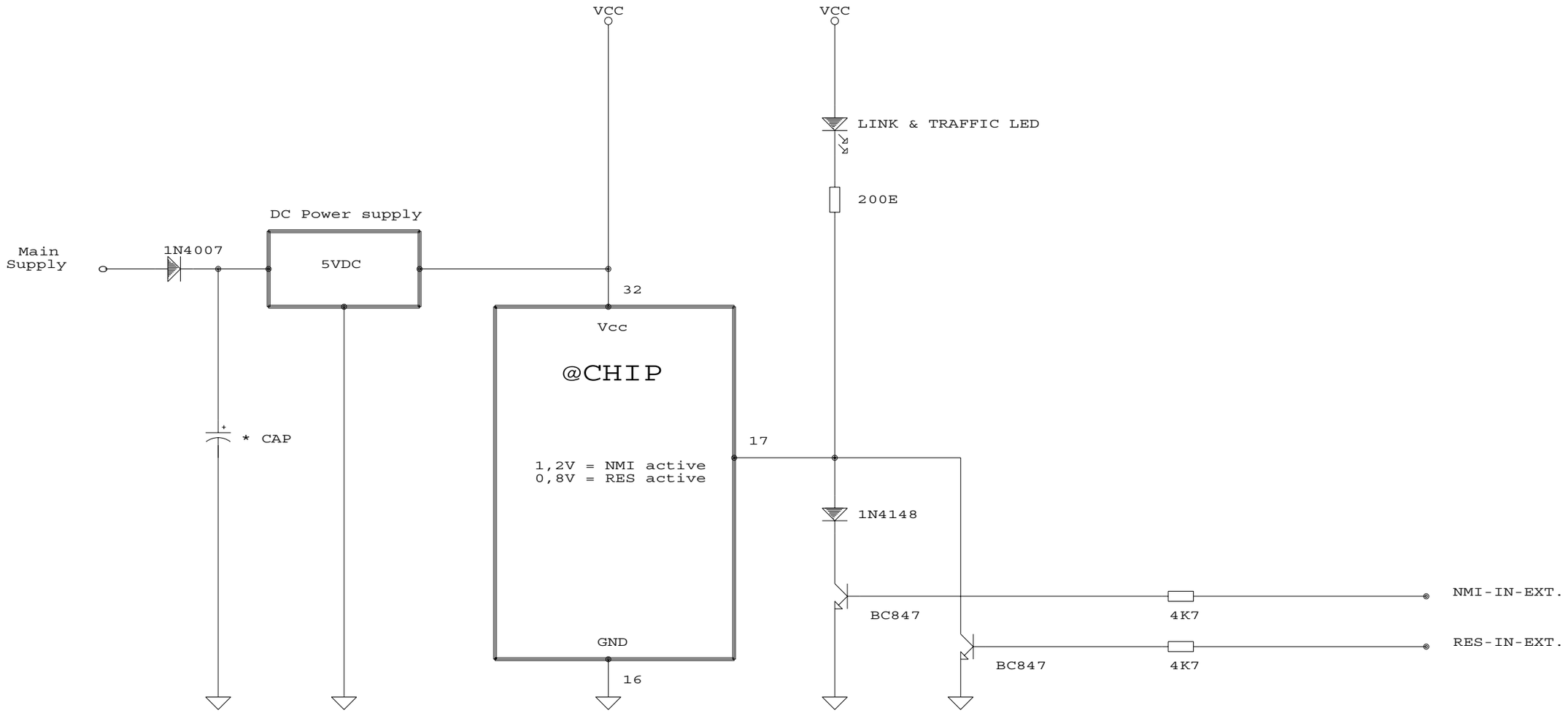
Title
IPC@CHIP SC12 PIN17-PFAIL/RES-OUT

Size	Document Number	REV
A3	(C) 1995 - 1999 SC12APL1	01
Date: November 16, 1999	Sheet 1 of 1	



NMI-IN-EXT = High active digital NMI - Input from any external Logic.
RES-IN-EXT = High active digital RES - Input from any external Logic.
* CAP = Value is dependent from the saveable amount of data.

Gez. : IB 16.11.99
Gepr.: JW 15.11.99

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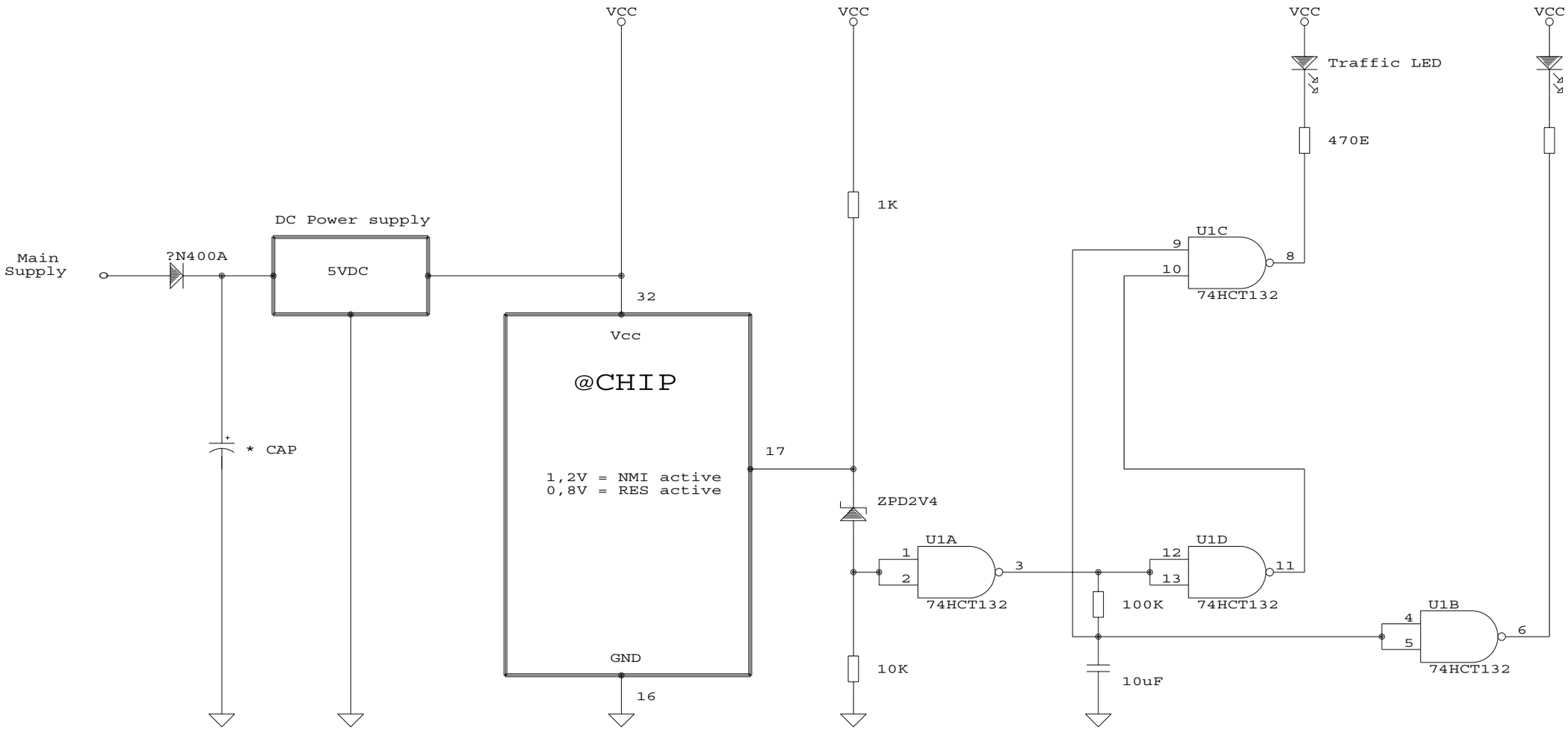
Title
IPC@CHIP SC12 PIN17 - NMI-IN/RES-IN

Size	Document Number	REV
A3	(C) 1995 - 1999 SC12APL2	01
Date: November 16, 1999	Sheet 1 of 1	



Gez. : IB 16.11.99

Gepr.: JW 15.11.99

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Title
IPC@CHIP SC12 PIN17-Link&Traffic LED separat

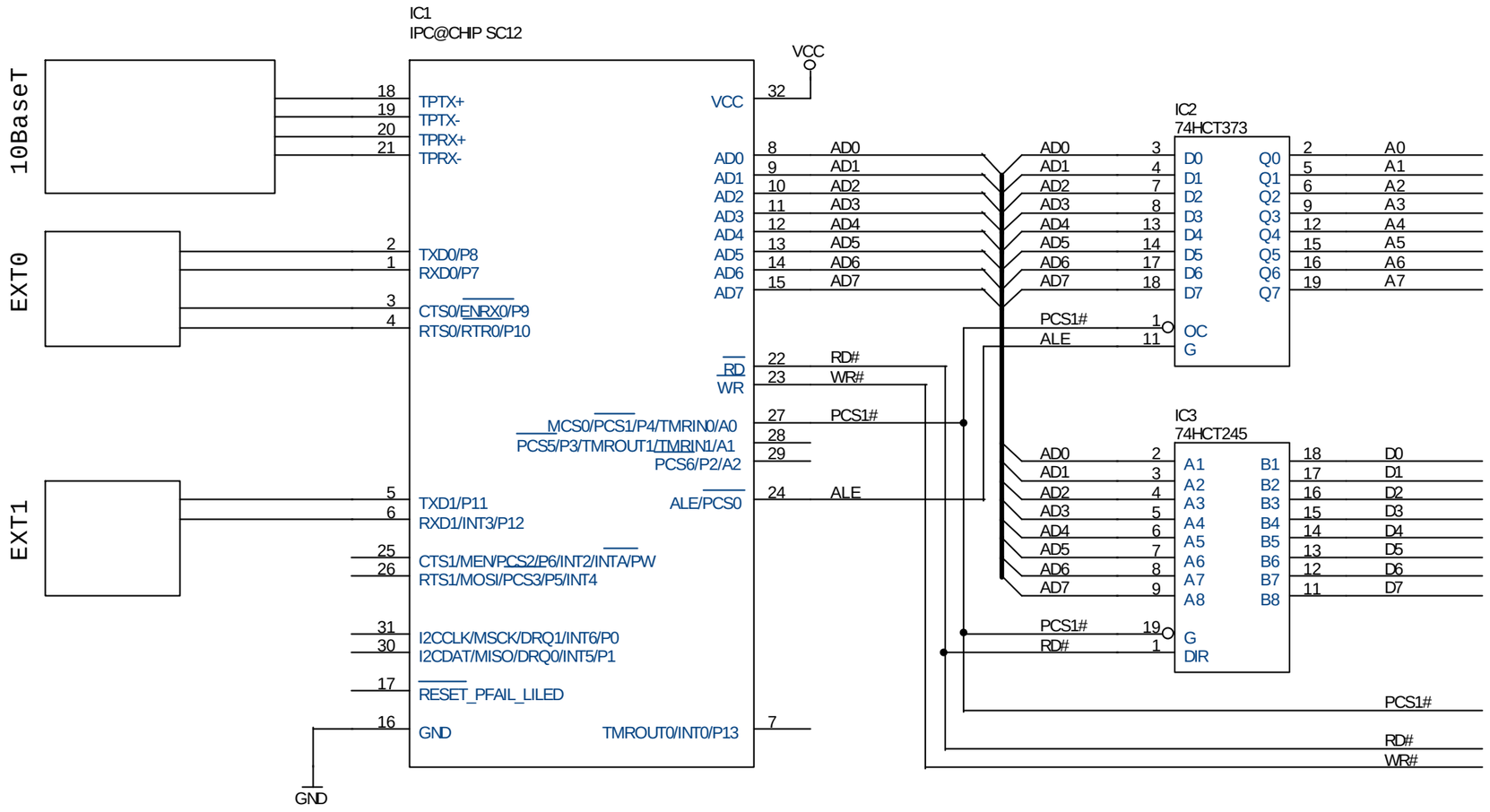
Size	Document Number	REV
A3	(C) 1995 - 1999 SC12APL3	01
Date: November 23, 1999	Sheet 1 of 1	

9. HOW TO CONNECT ?

The following pages contain schematics, that show different kind of ICs connected to the IPC@CHIP® family microcontroller.

Attention: These circuit examples are unevaluated! They will give you hints how to connect different kind of ICs in different manner to the IPC@CHIP® family microcontroller.

256 x 8bit I/O-Extension



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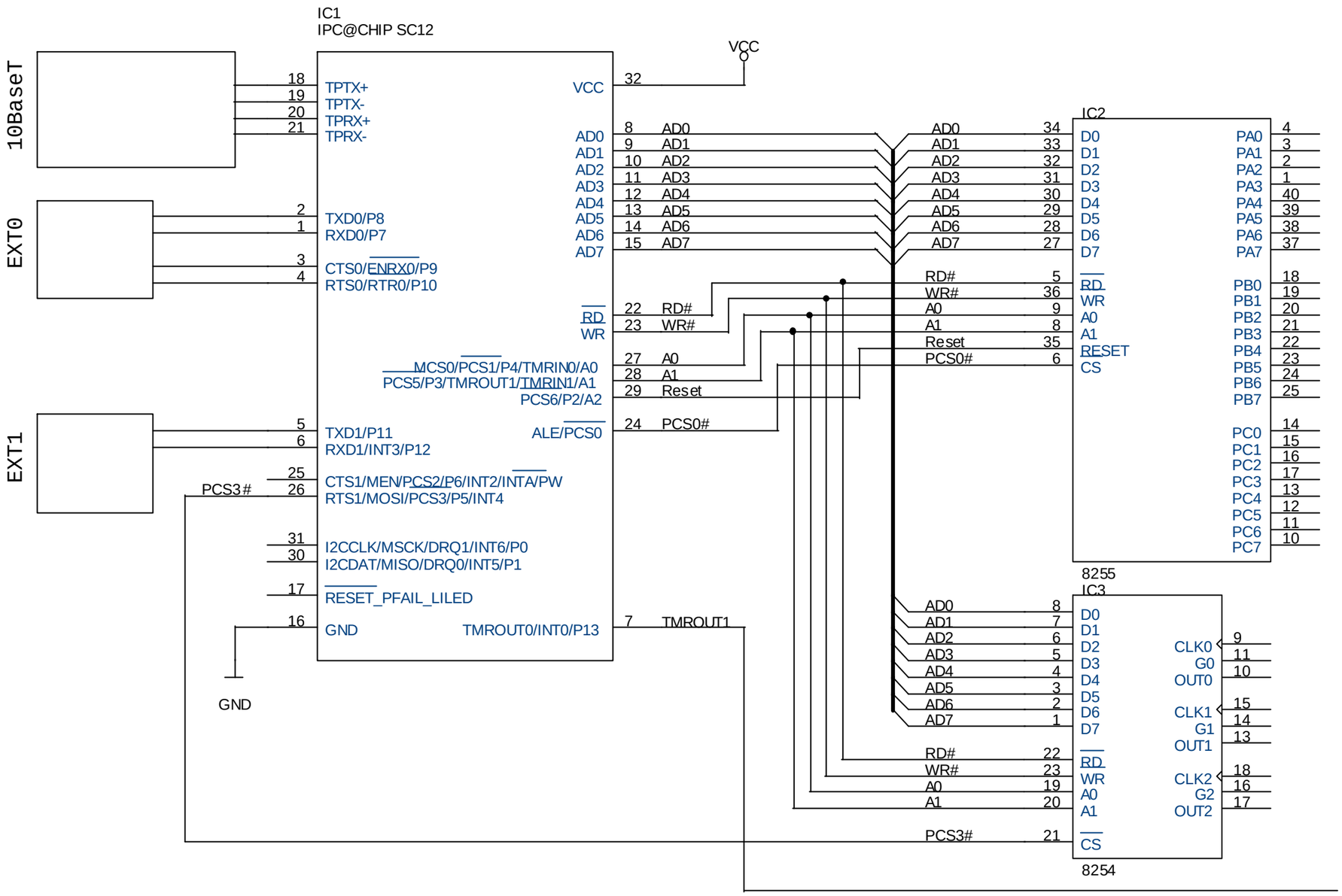
Title: IPC@CHIP SC12 circuit example		
Size: A4	Document Number: (c) 1996 - 99 CHIPD1	Rev: 0.5
Date: Tuesday, November 23, 1999	Sheet 1 of 1	

8255 24 bit I/O-Extension and 8254 Timer/Counter



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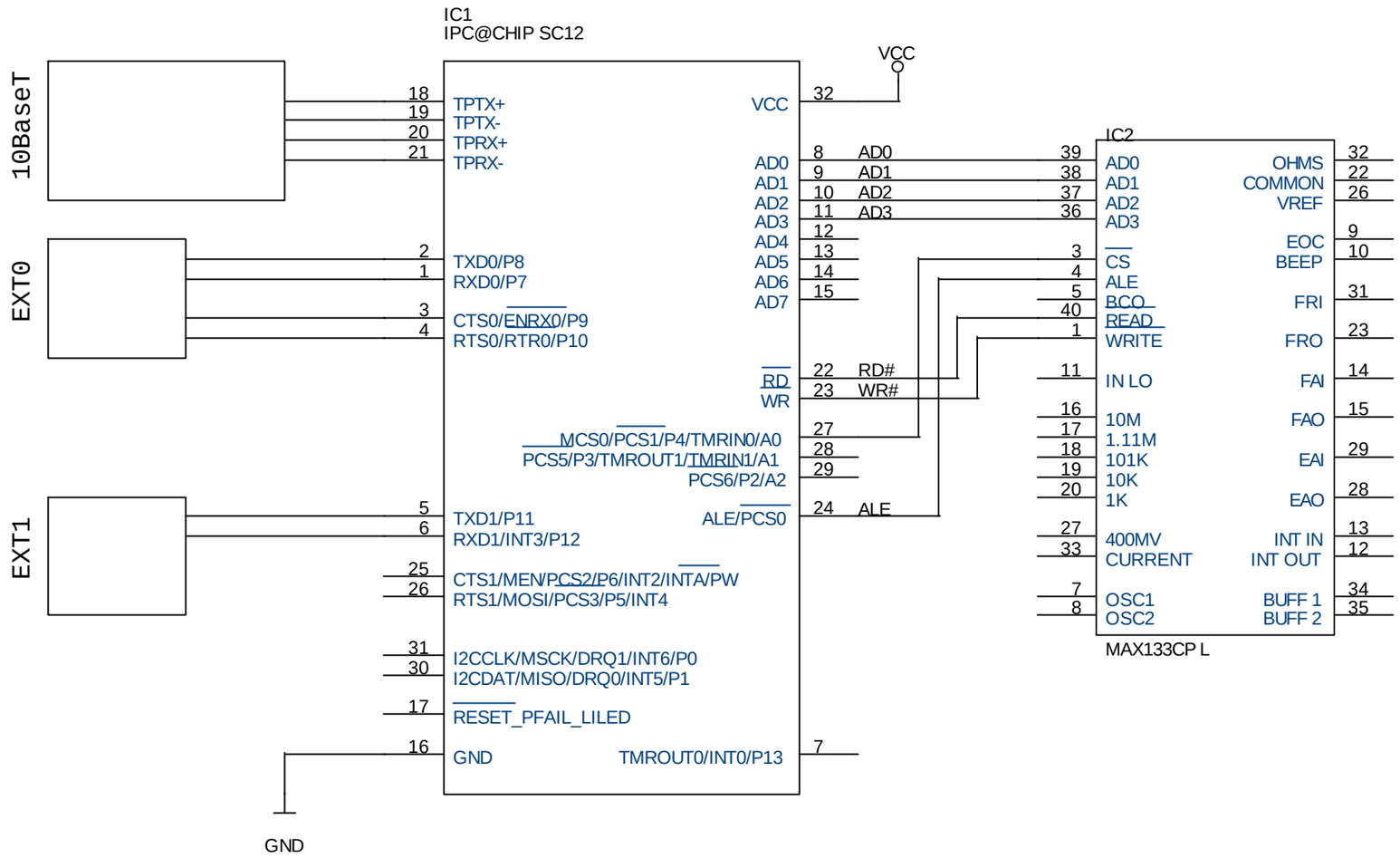
Title: IPC@CHIP SC12 circuit example		
Size: A4	Document Num ber: (c) 1996 - 99 CHIP D1	Rev: 0.5
Date: Tuesday, November 23, 1999	Sheet 1 of 1	

Multimeter ADC MAX133CPL



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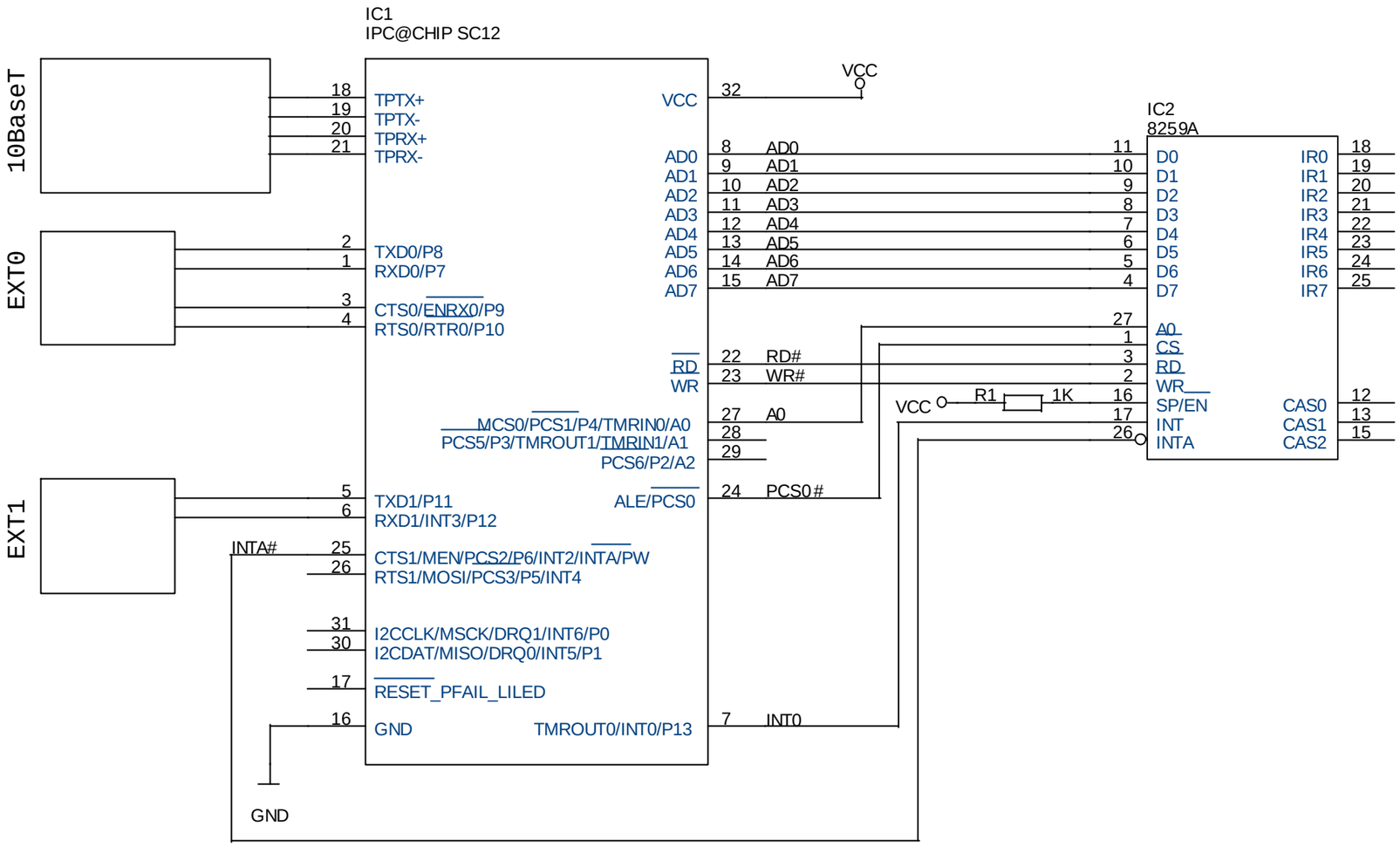
Title	IPC@CHIP SC12 circuit example	
Size A4	Document Num ber (c) 1996 - 99 CHI PD1	Rev 0.5
Date: Tuesday, November 23, 1999	Sheet 1 of 1	

8259 peripheral interrupt controller



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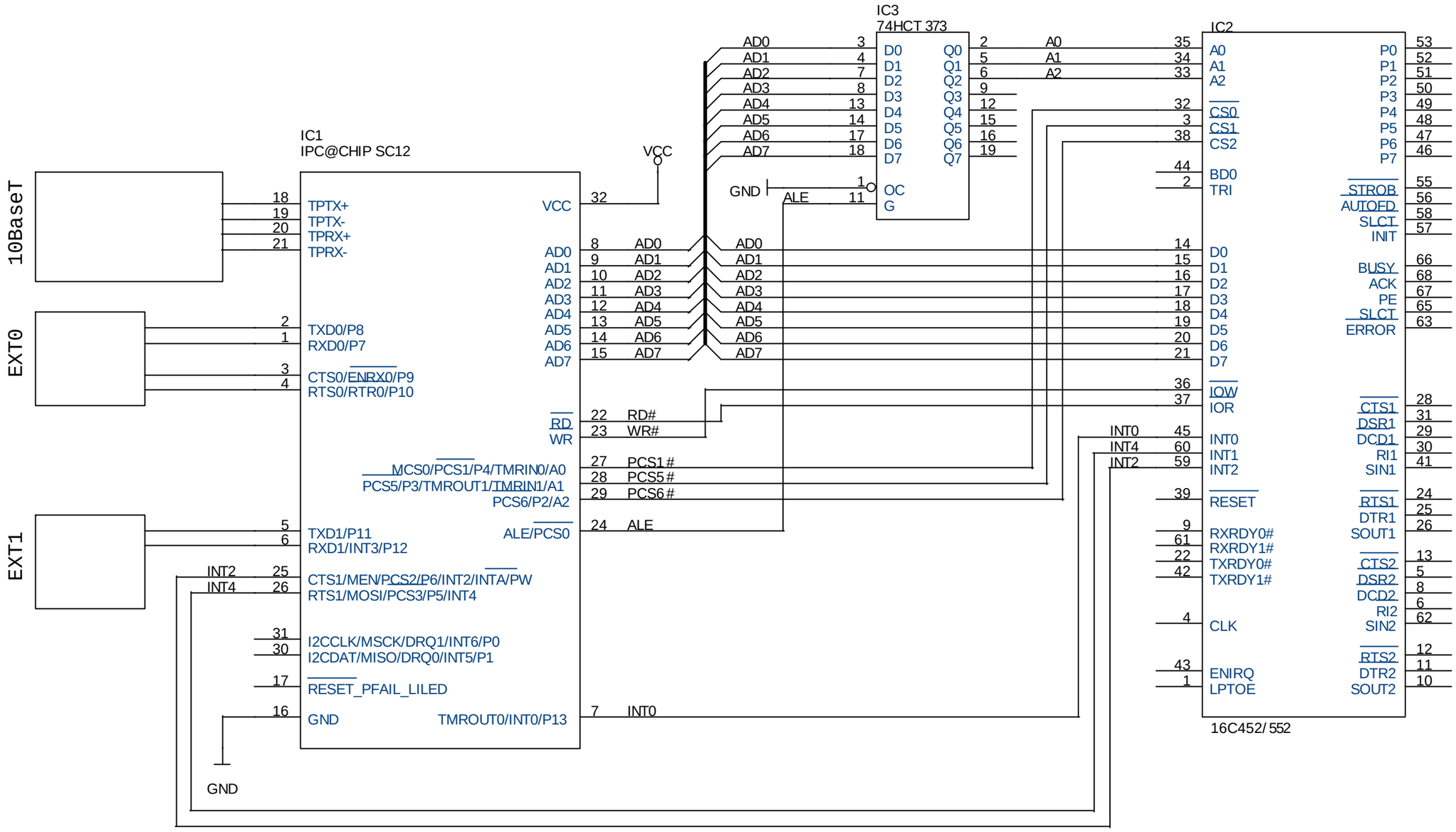
Title	IPC@CHIP SC12 circuit example	
Size A4	Document Number (c) 1996 - 99 CHIP D1	Rev 0.5
Date: Tuesday, November 23, 1999	Sheet 1 of 1	

16C452/552 2 UART with FIFO and Printer Port



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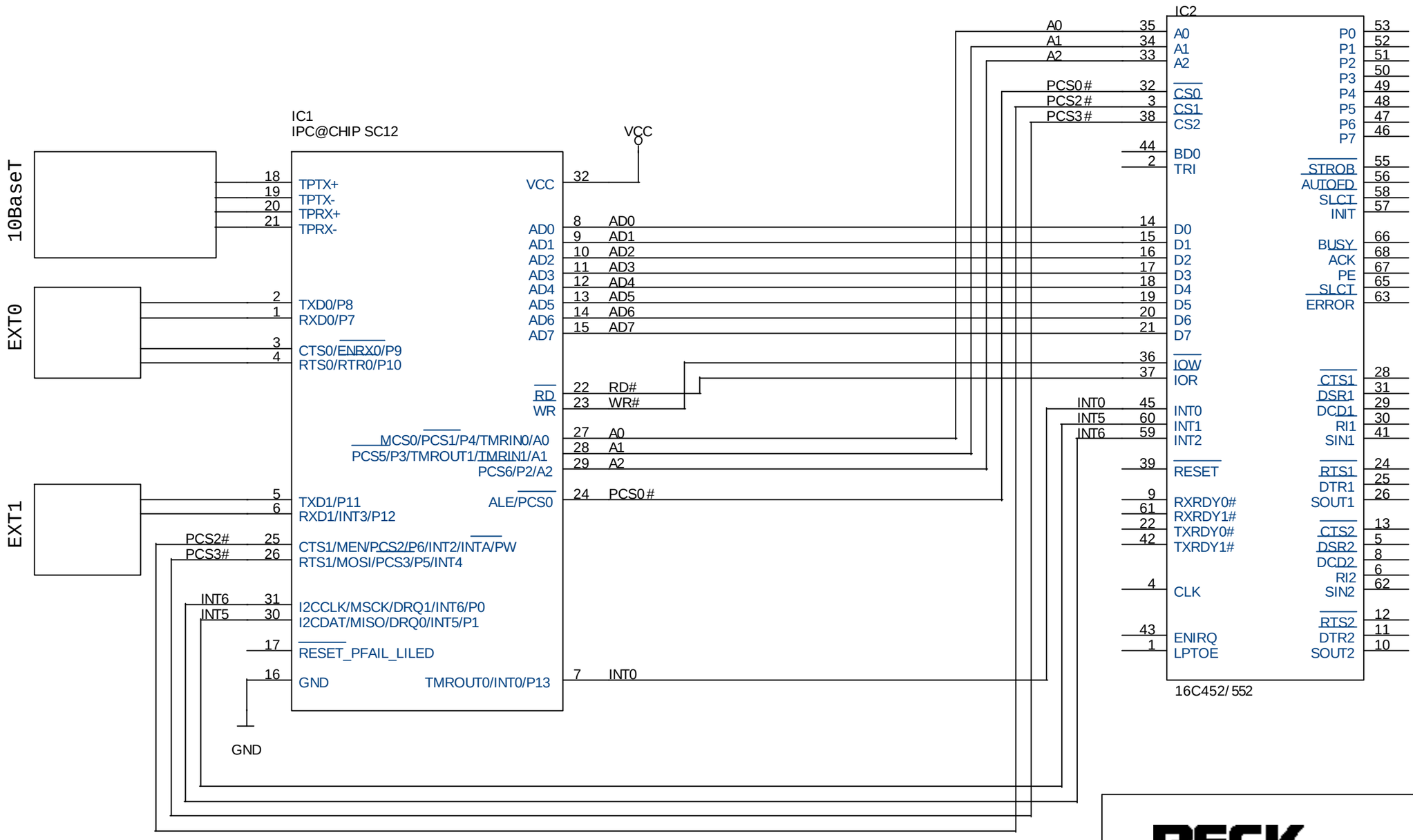
Title	IPC@CHIP SC12 circuit example	
Size: A4	Document Num ber: (c) 1996 - 99 CHIP D1	Rev: 0.5
Date: Tuesday, November 23, 1999	Sheet 1 of 1	

16C452/552 2 UART with FIFO and Printer Port



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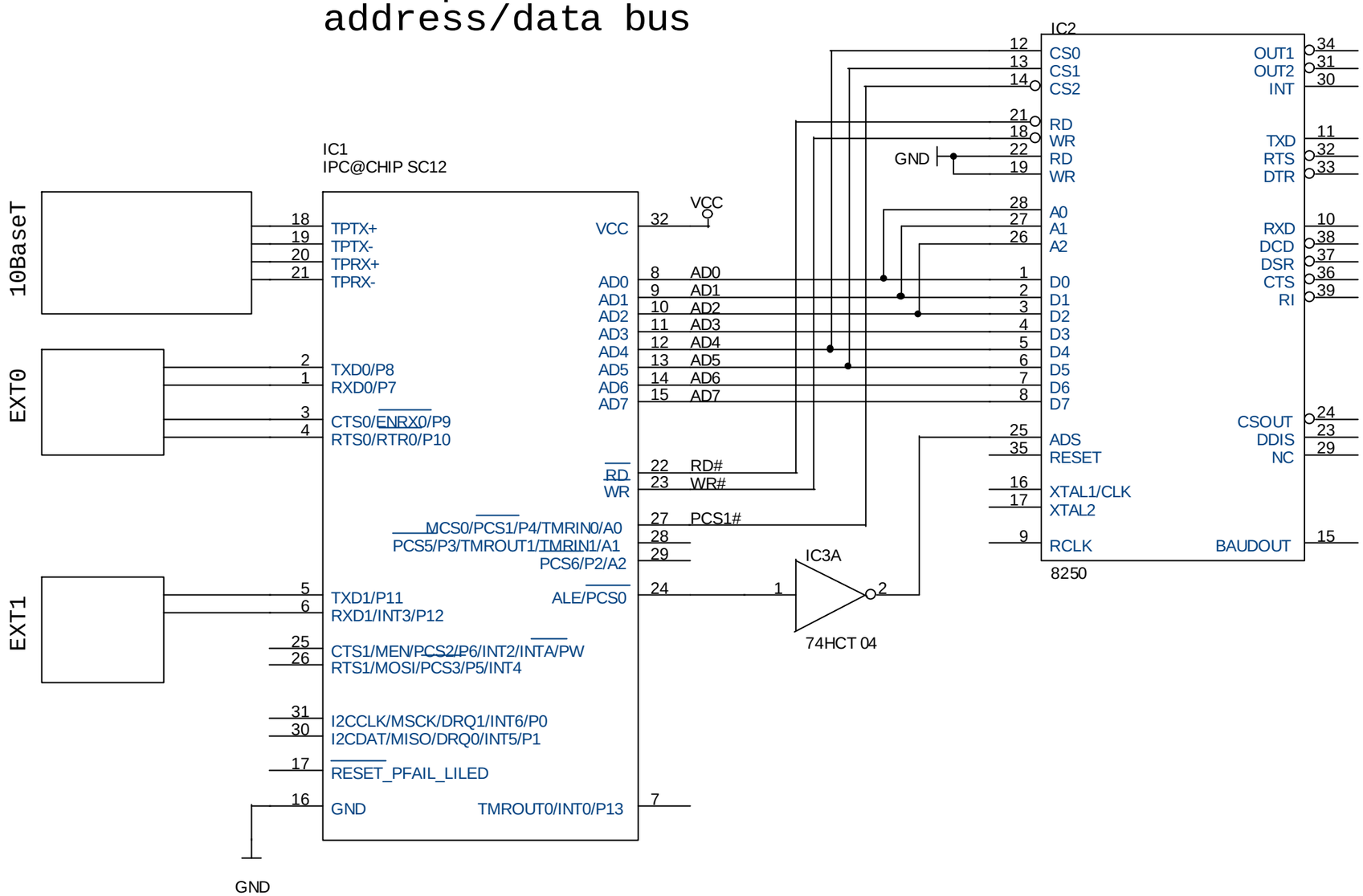
Title	IPC@CHIP SC12 circuit example	
Size: A4	Document Num ber: (c) 1996 - 99 CHIP D1	Rev: 0.5
Date: Tuesday, November 23, 1999	Sheet 1 of 1	

UART 8250 with multiplexed address/data bus



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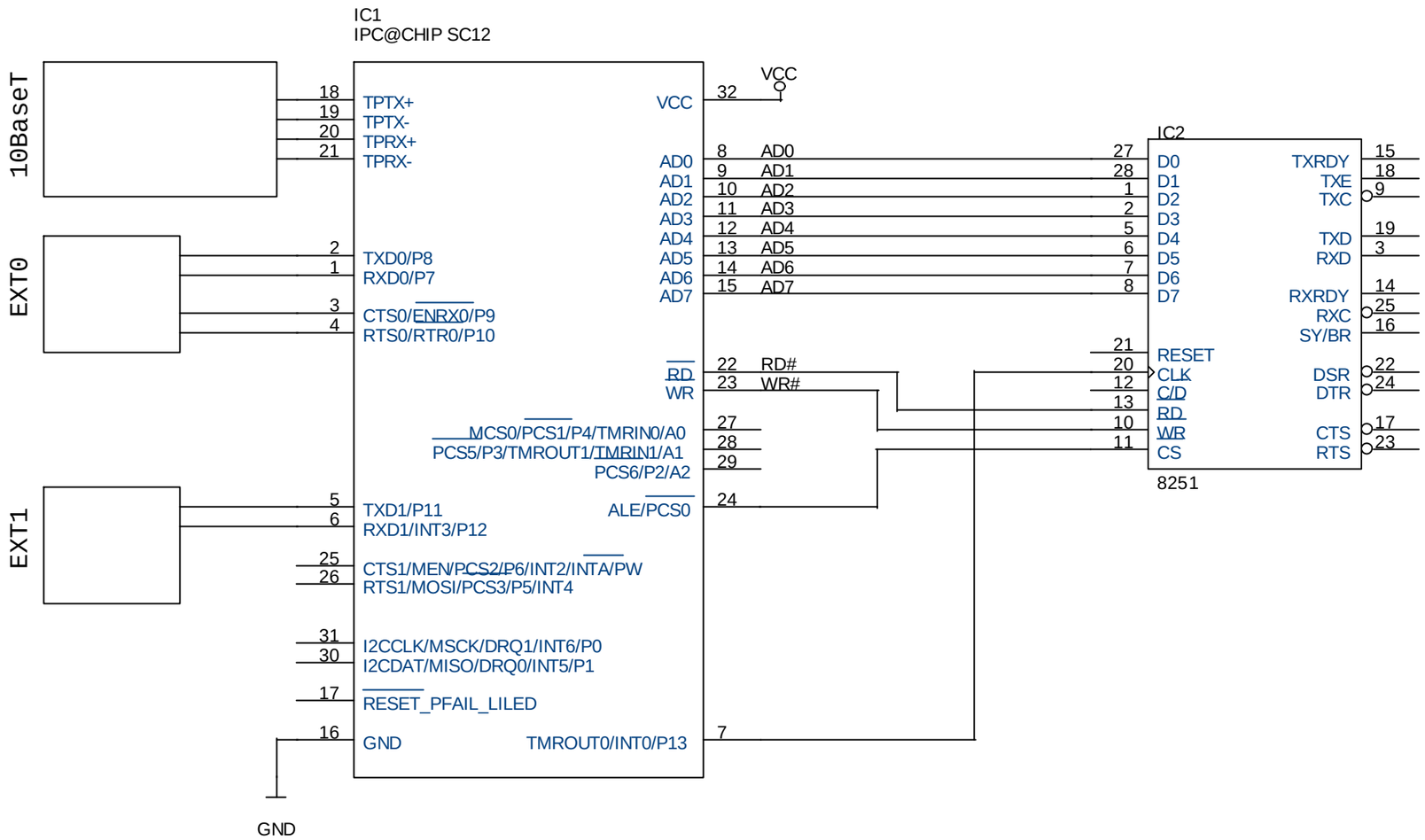
Title	IPC@CHIP SC12 circuit example
Size: A4	Document Num ber: (c) 1996 - 99 CHIP D1 — Rev: 0.5
Date: Tuesday, November 23, 1999	Sheet 1 of 1

UART 8251



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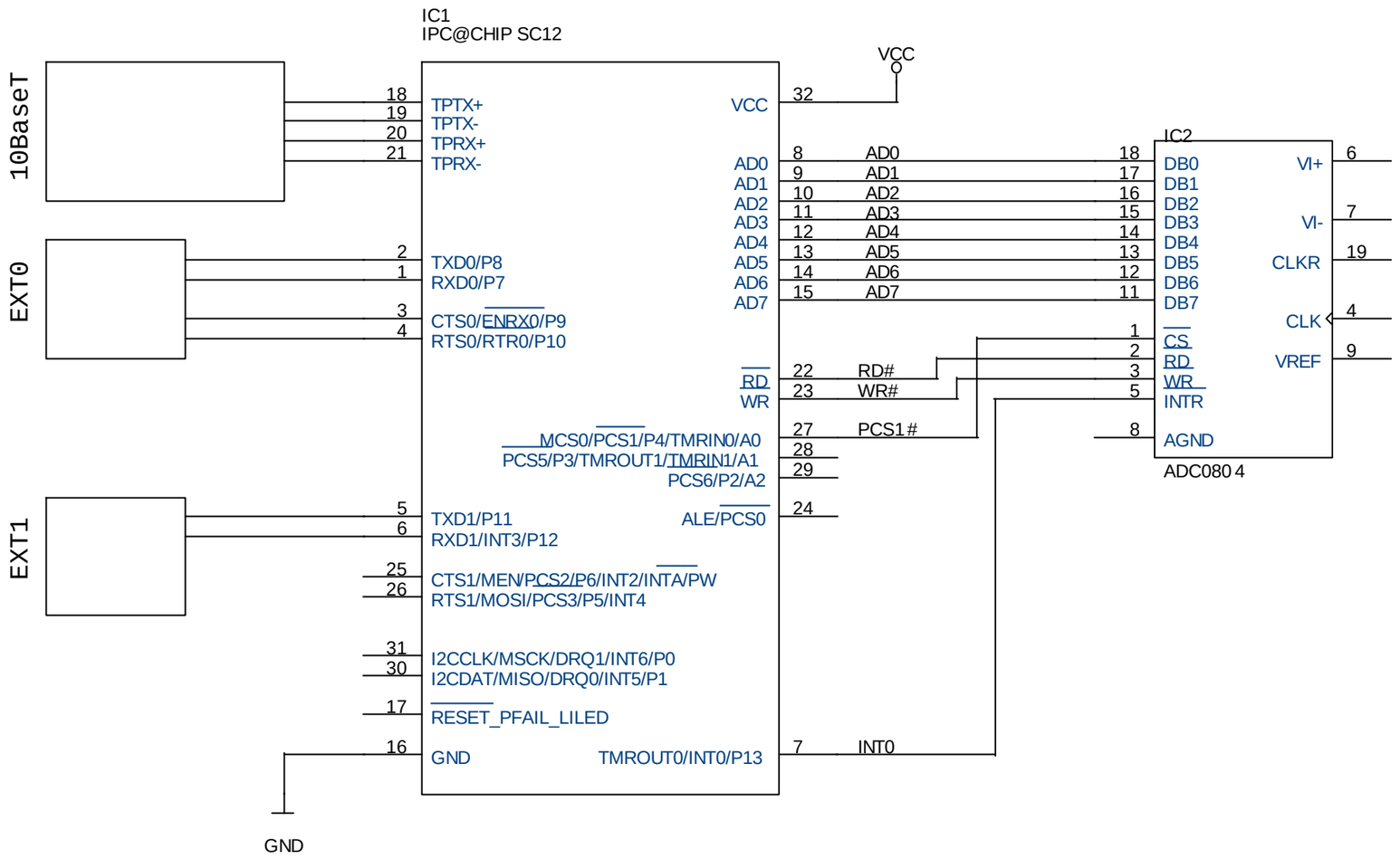
Title

IPC@CHIP SC12 circuit example

Size	Document Numb er	Rev
A4	(c) 1996 - 99 CHIP D1	0.5
Date: Tuesday, November 23, 1999	Sheet 1 of 1	

low-cost 8bit ADC



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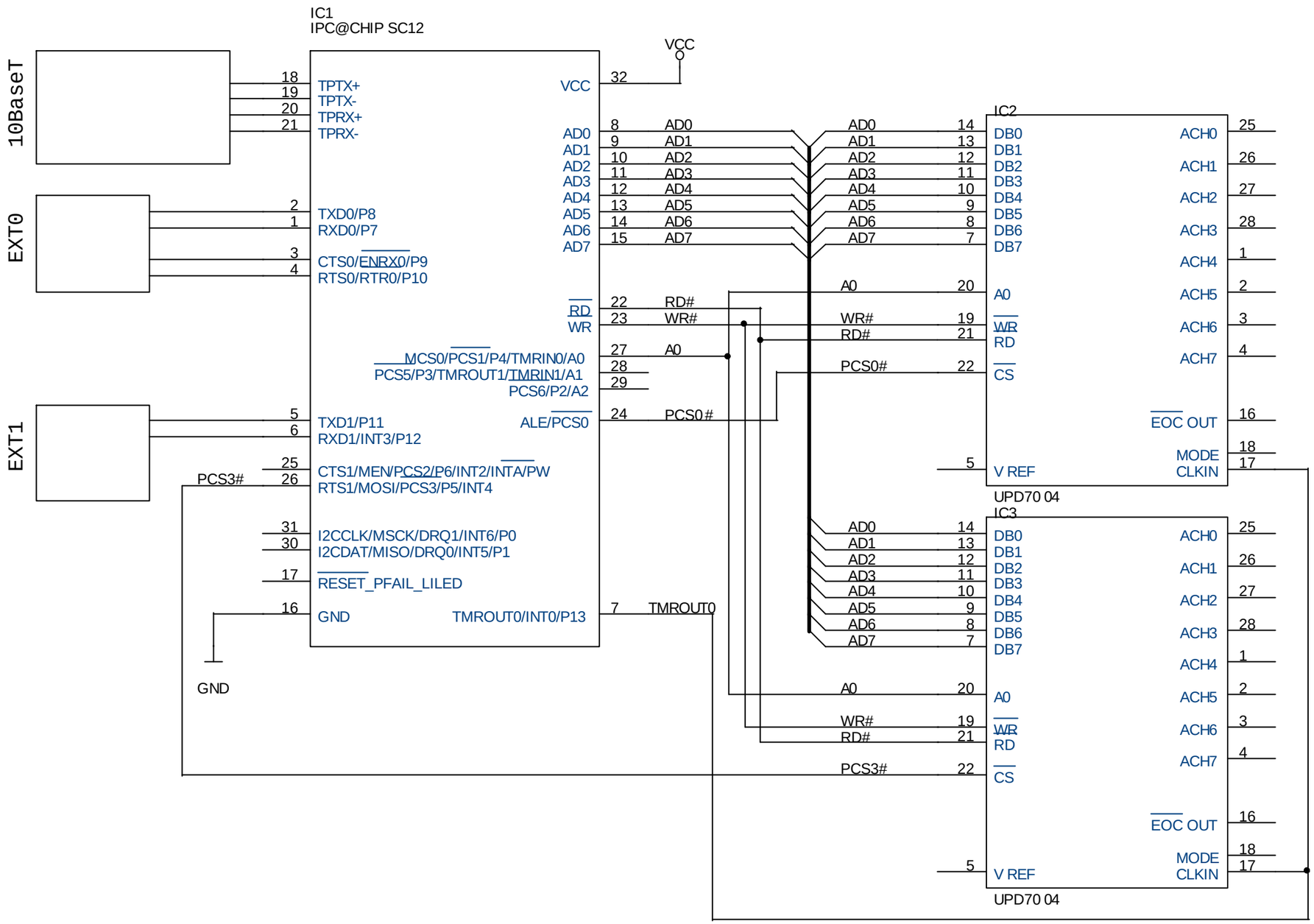
Title	IPC@CHIP SC12 circuit example
Size: A4	Document Number: (c) 1996 - 99 CHIPDI
Rev: 0.5	
Date: Tuesday, November 23, 1999	Sheet 1 of 1

16x 10bit ADC with 2x µPD7004



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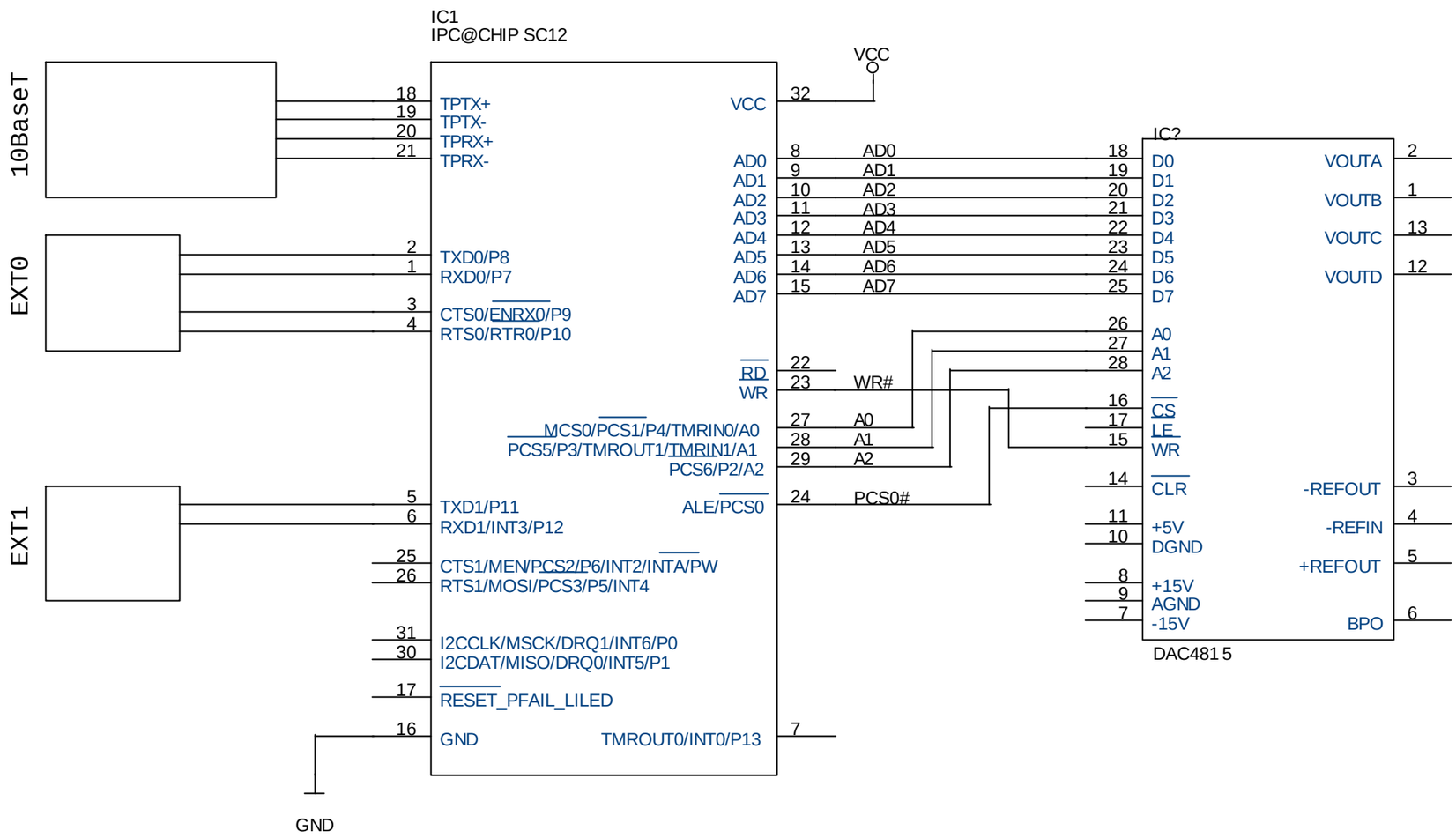
Title	IPC@CHIP SC12 circuit example	
Size: A4	Document Num ber: (c) 1996 - 99 CHIP D1	Rev: 0.5
Date: Tuesday, November 23, 1999	Sheet 1 of 1	

DAC4815 4x 12bit



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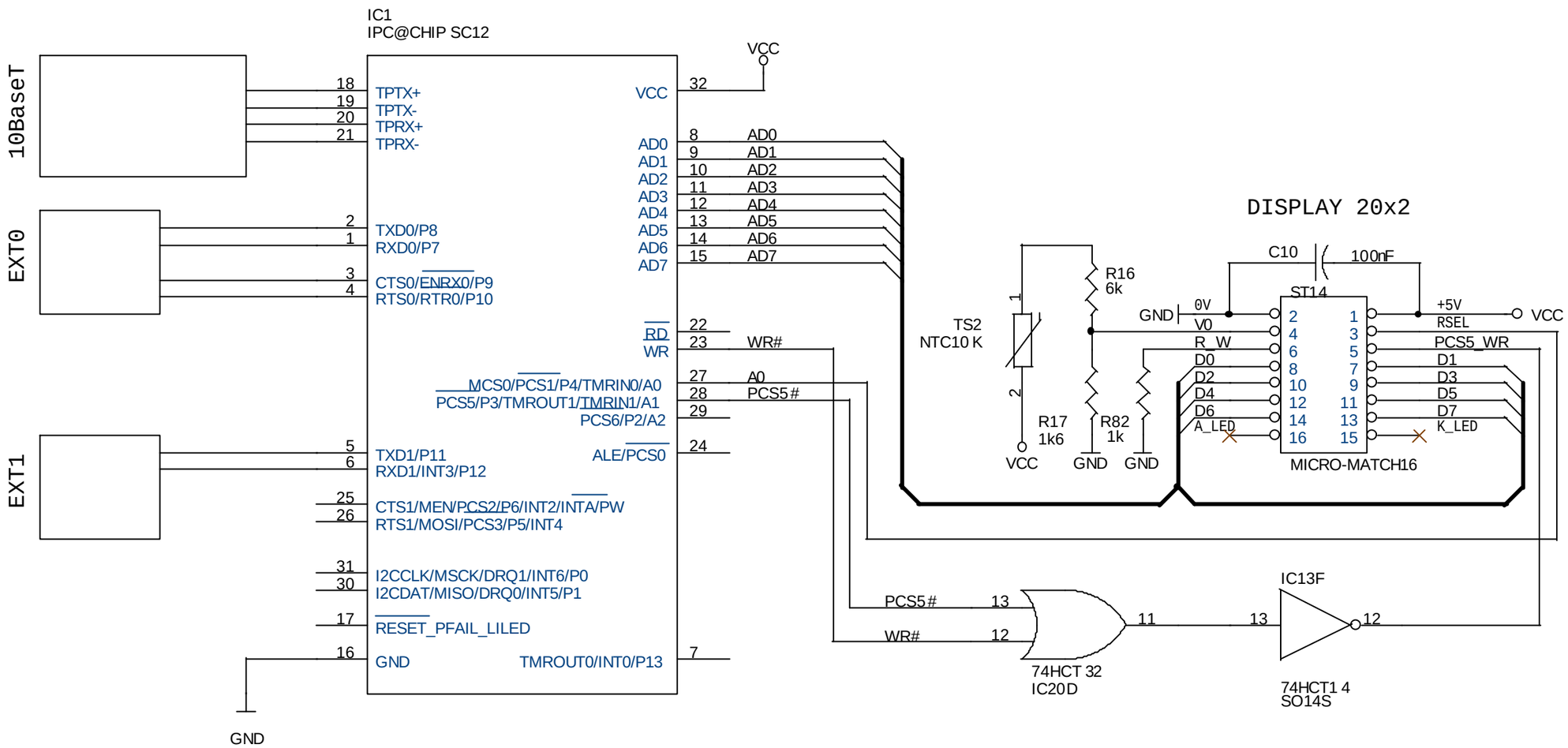
Title: IPC@CHIP SC12 circuit example		
Size: A4	Document Num ber: (c) 1996 - 99 CHIP D1	Rev: 0.5
Date: Tuesday, November 23, 1999	Sheet 1 of 5	

LC-Display



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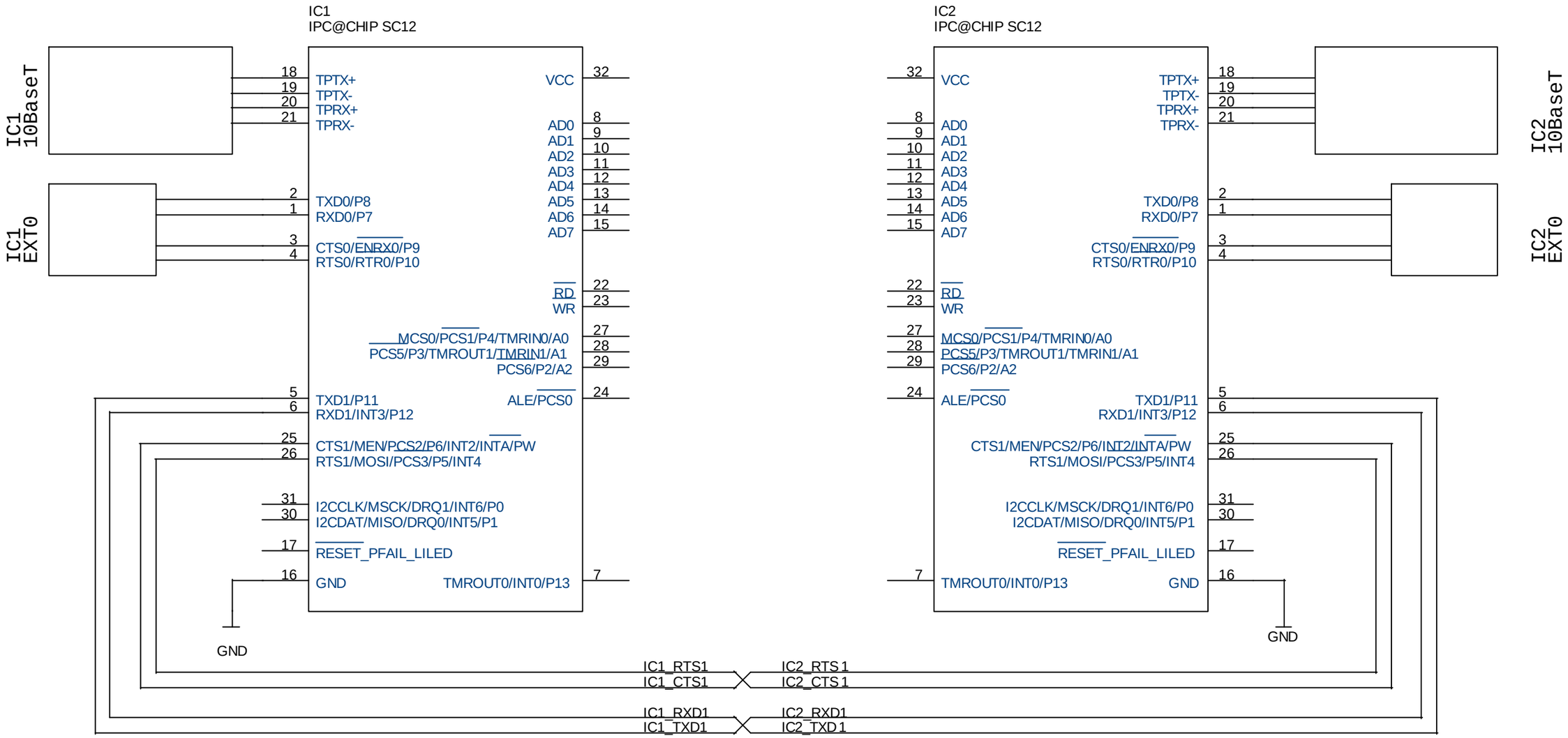
Title	IPC@CHIP SC12 Beschaltungsbeispiel	
Size A4	Document Num ber (c) 1996 - 99 CHIP D1	Rev 0.5
Date: Tuesday, November 23, 1999	Sheet 1 of 1	

Ethernet to Ethernet Router



high speed communication
with serial port DMA

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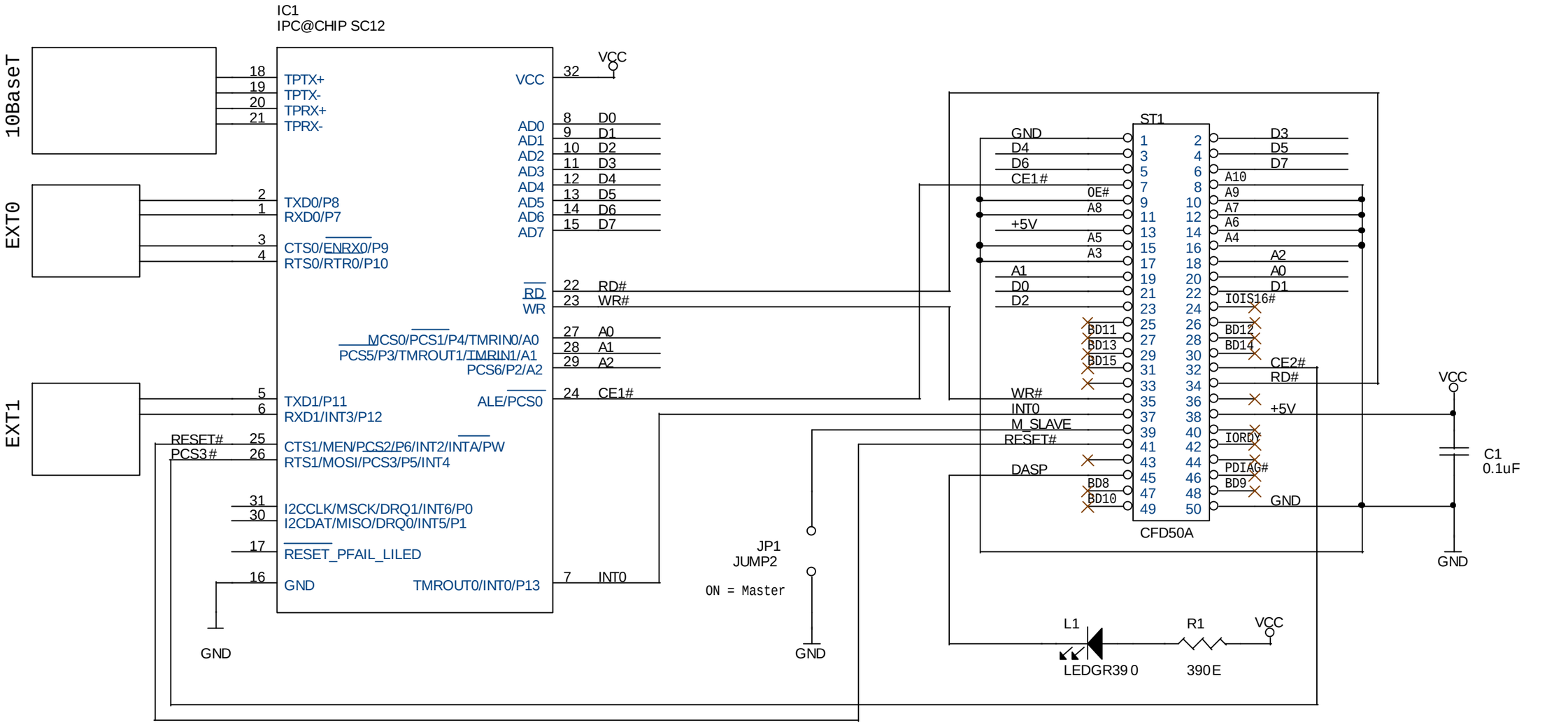
Title: IPC@CHIP SC12 circuit example		
Size: A4	Document Number: (c) 1996 - 99 CHIP D1	Rev: 0.5
Date: Tuesday, November 23, 1999	Sheet 1 of 1	

8bit compact flash disk



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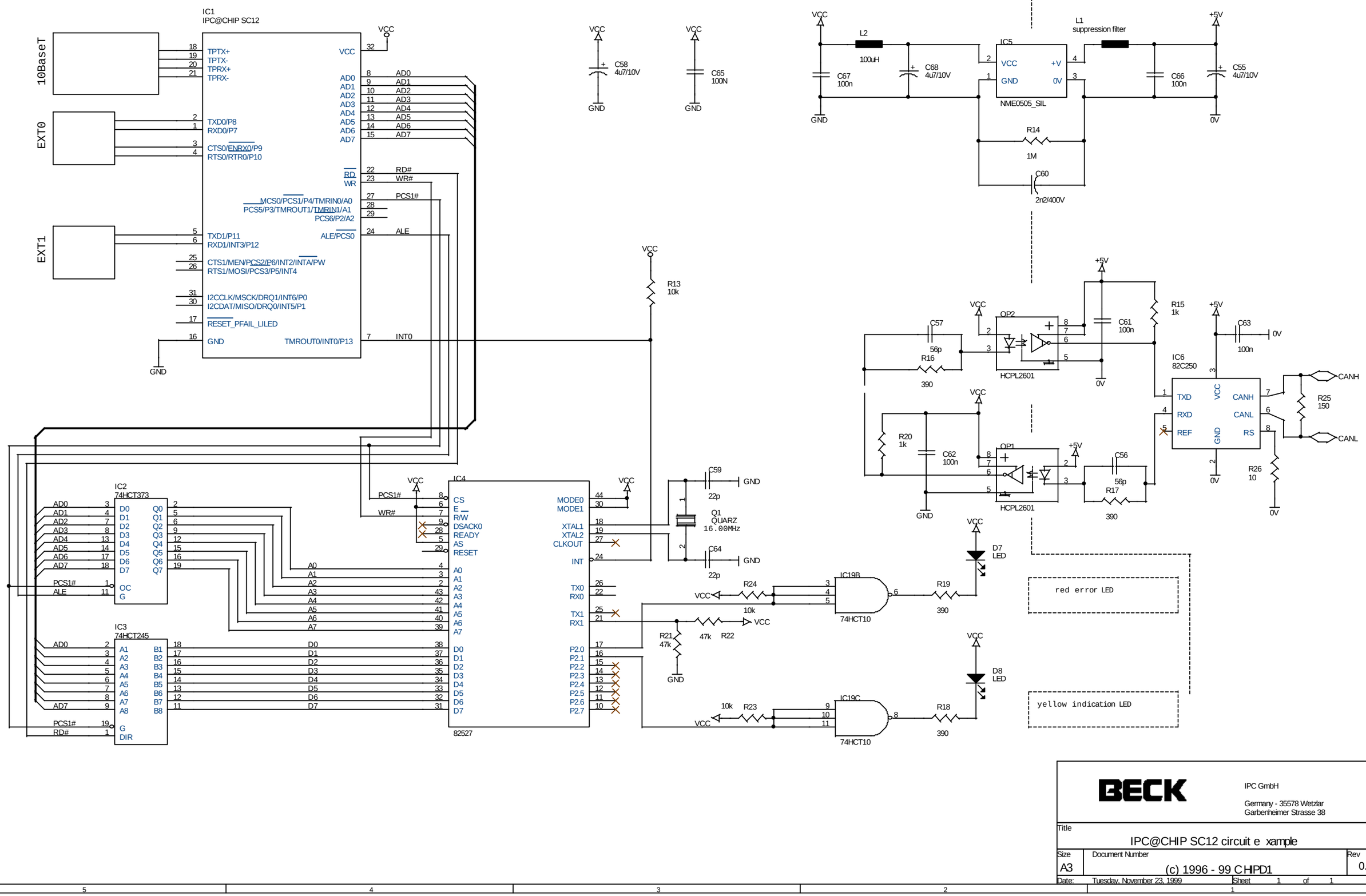
Title	IPC@CHIP SC12 circuit example	
Size A4	Document Numb er (c) 1996 - 99 CHIP D1	Rev 0.5
Date: Tuesday, November 23, 1999	Sheet 1 of 1	

82527 CAN bus master



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Title	IPC@CHIP SC12 circuit e xample	
Size: A3	Document Number: (c) 1996 - 99 CHIPD1	Rev: 0.5
Date: Tuesday, November 23, 1999	Sheet 1 of 1	